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**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

In re Application of

Richard D. Baertsch et al.

Serial No.: 09/774,530

Filed: January 31, 2001

For: DETECTOR FRAMING NODE  
ARCHITECTURE TO  
COMMUNICATE IMAGE DATA

:

:

: Group Art Unit: 2878

: Examiner:

: Attn: Official Draftsman

: Allowed Date:

: Issue Batch No.

To the Assistant Commissioner for Patents

**TRANSMITTAL OF FORMAL DRAWINGS**

Enclosed please find 53 sheet(s) of formal drawings for the above-identified patent  
application.

Respectfully submitted,

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Schenectady, New York

Date June 11, 2001

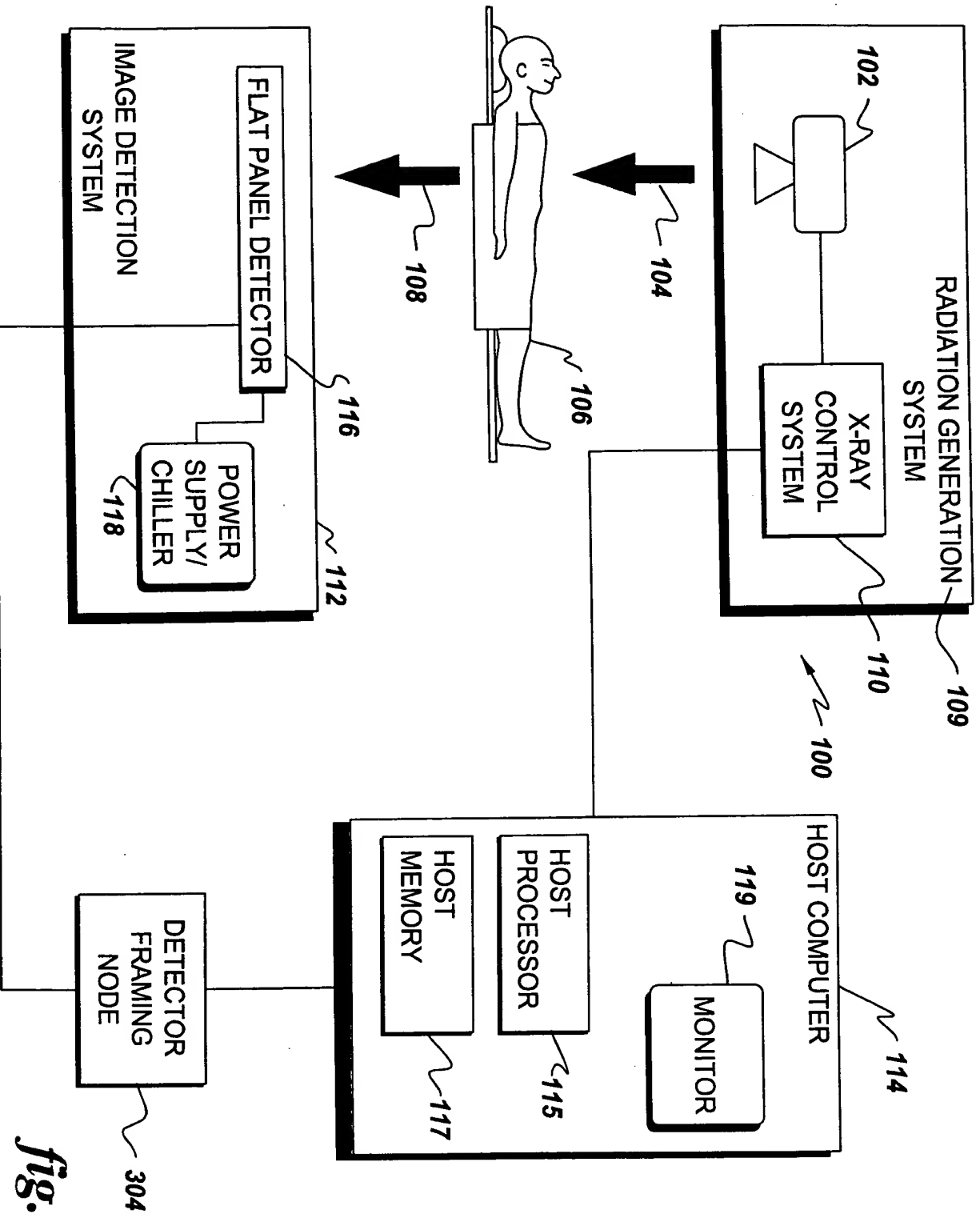
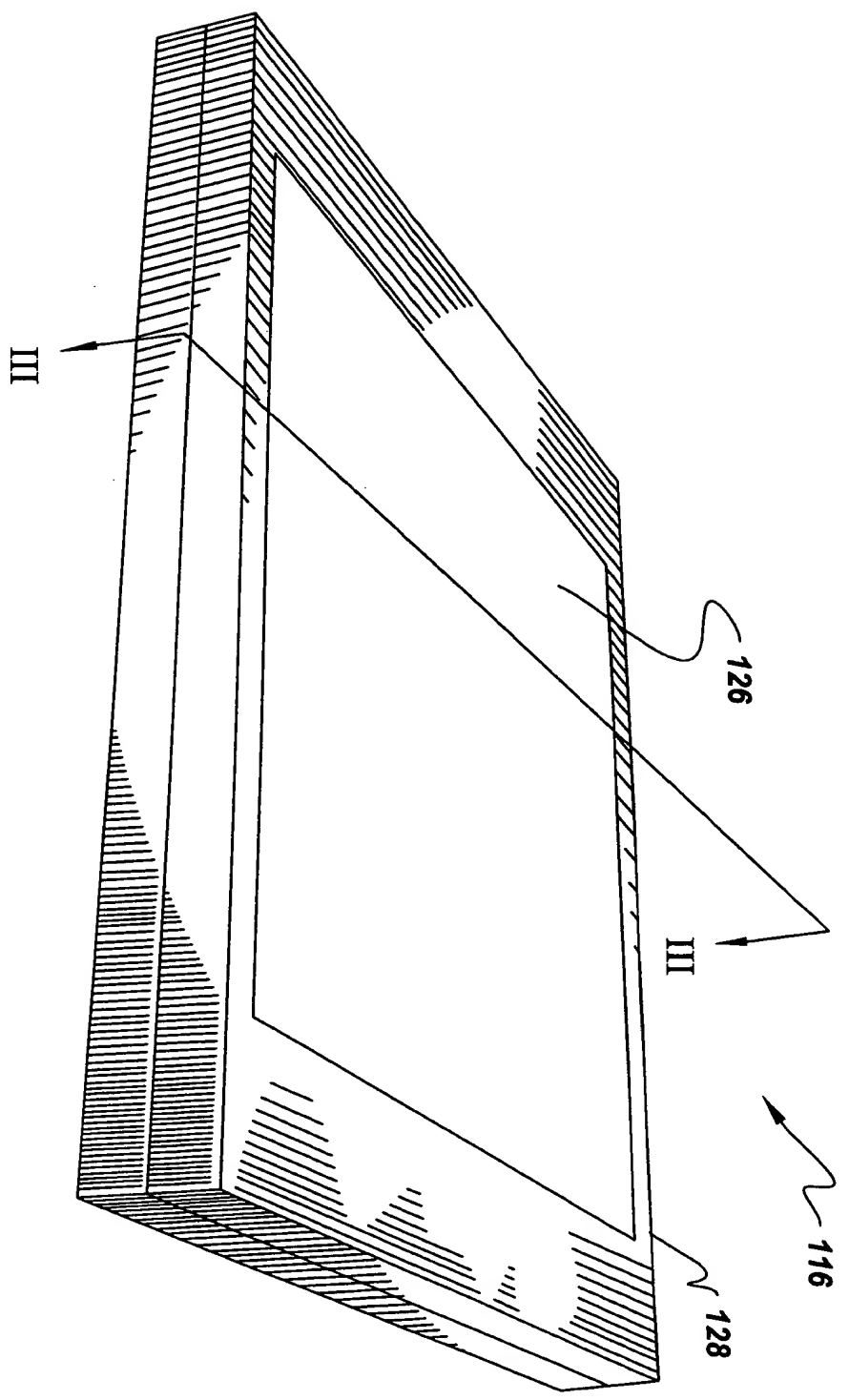


fig. 1



**fig. 2**  
(PRIOR ART)

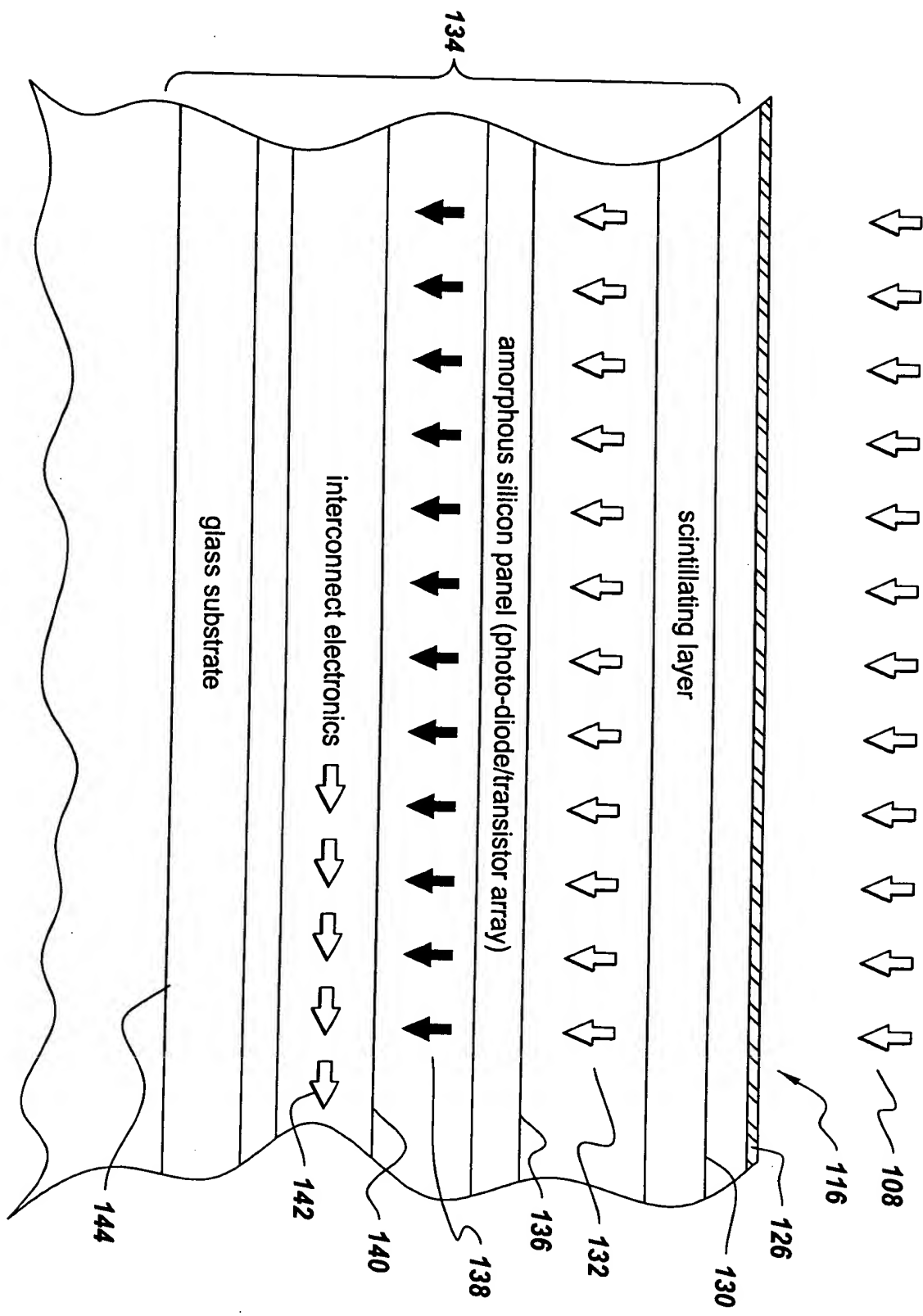
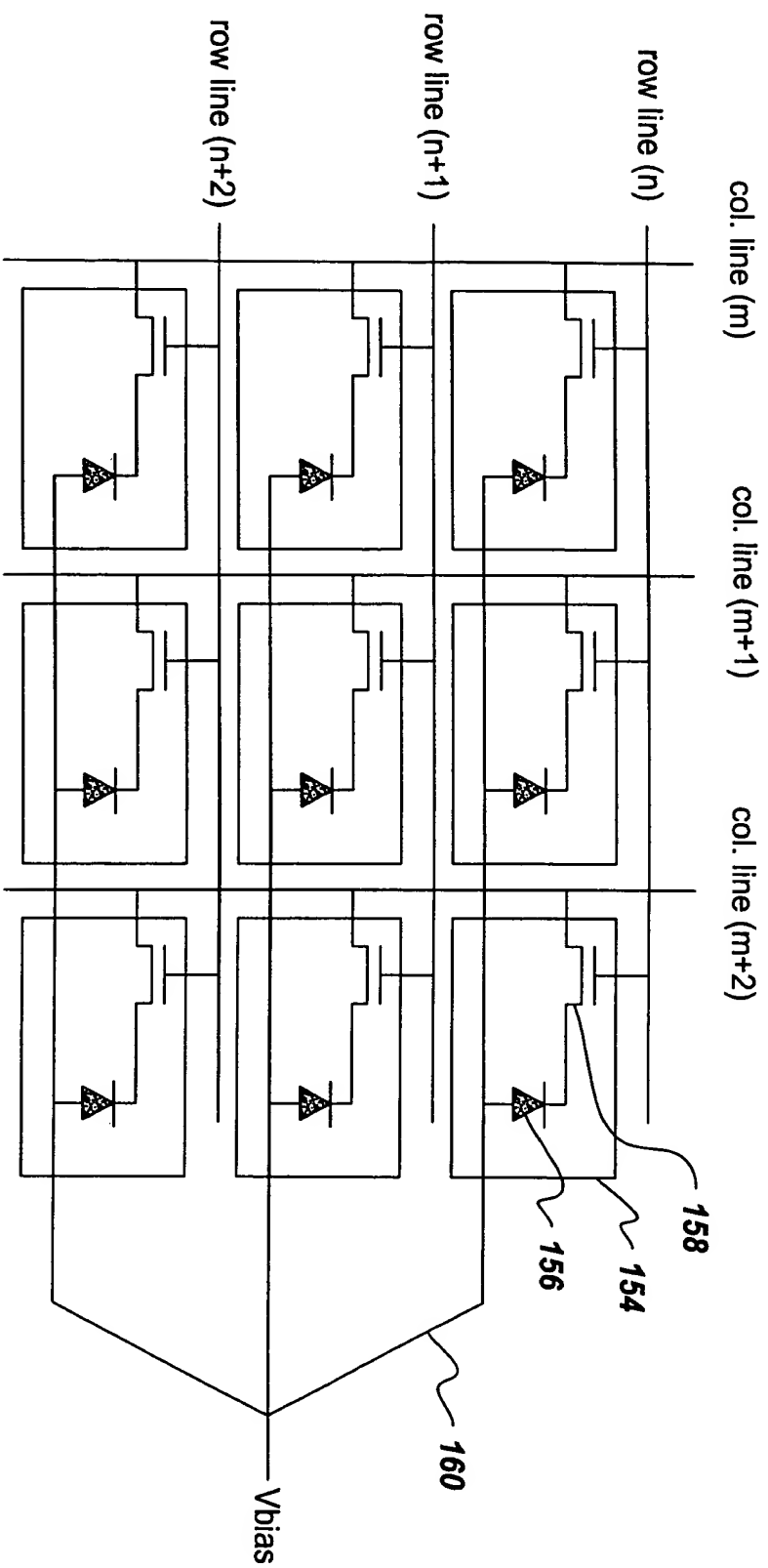


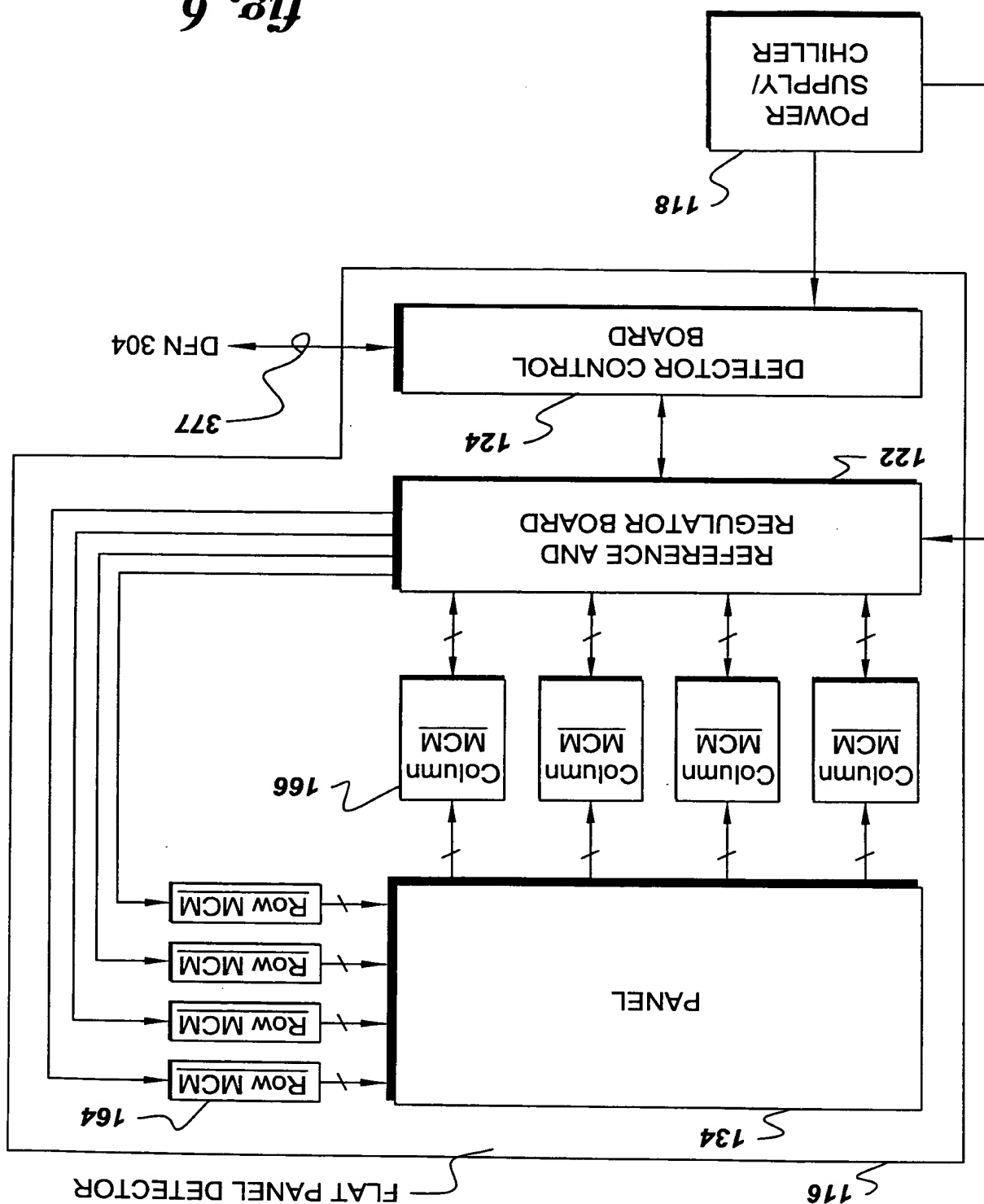
fig. 3



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**fig. 5**  
(Prior Art)



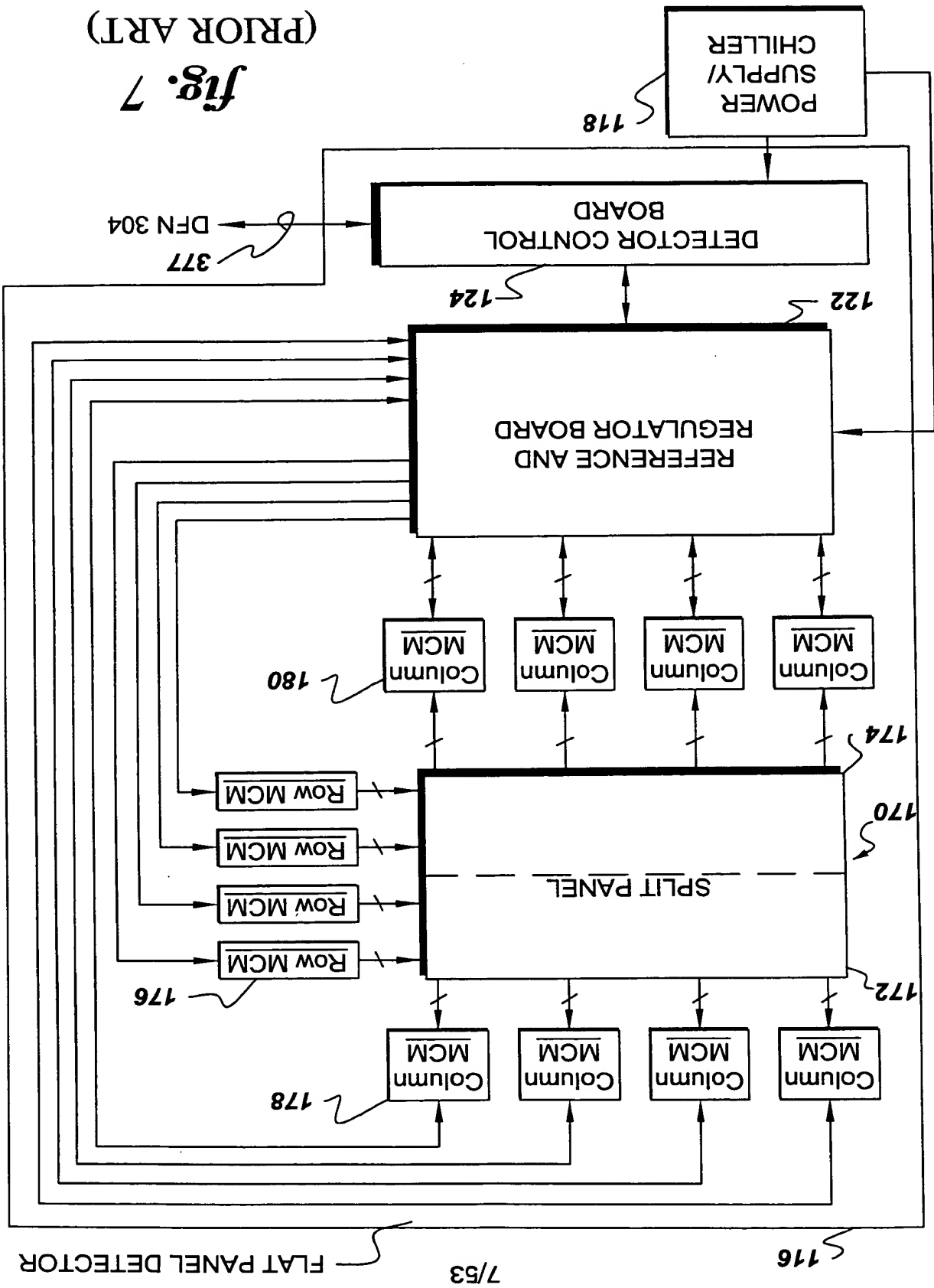


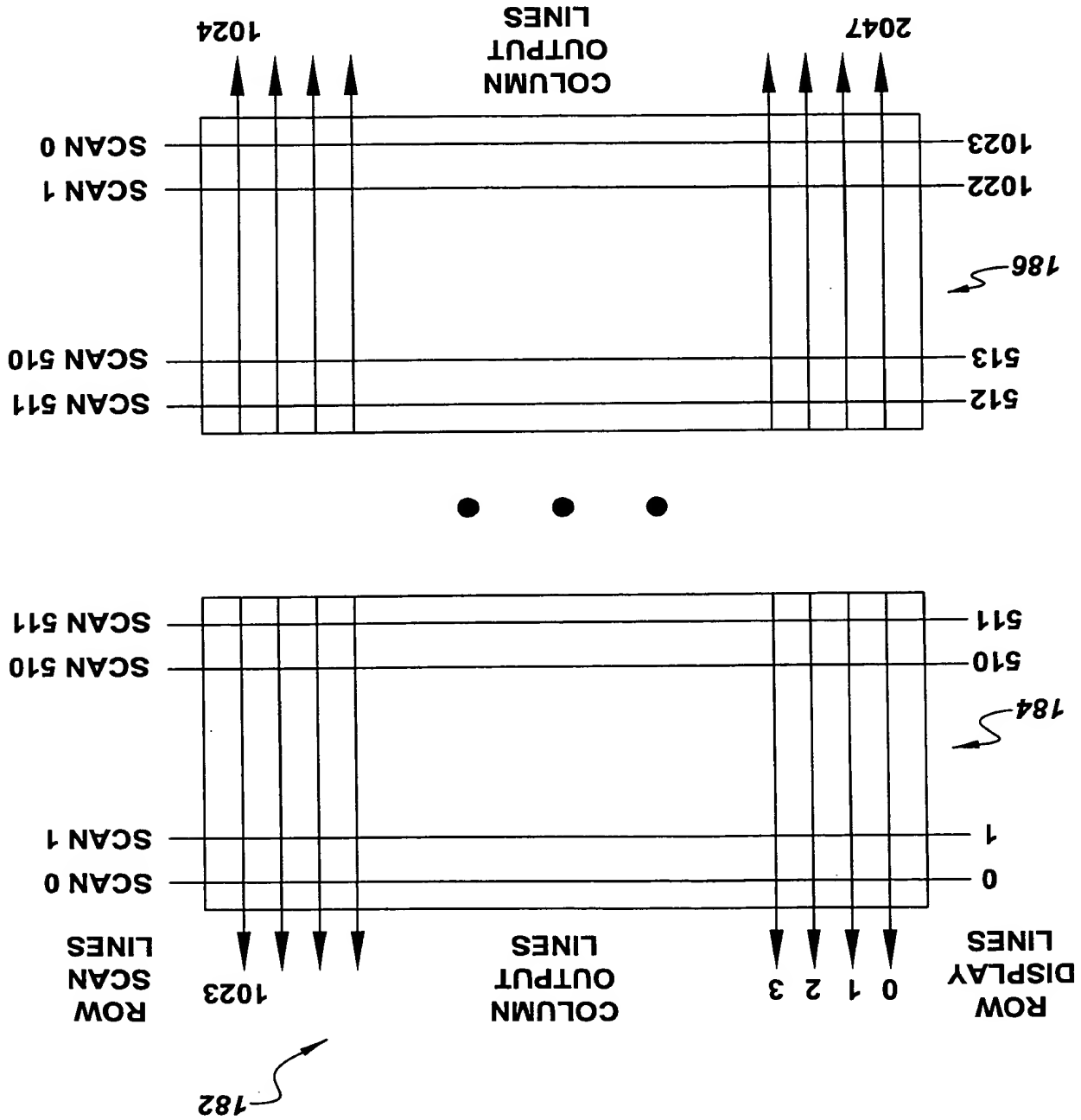
fig. 7 (PRIOR ART)



(PRIOR ART)

fig. 8

CARDIAC/SURGICAL DIGITAL X-RAY PANEL



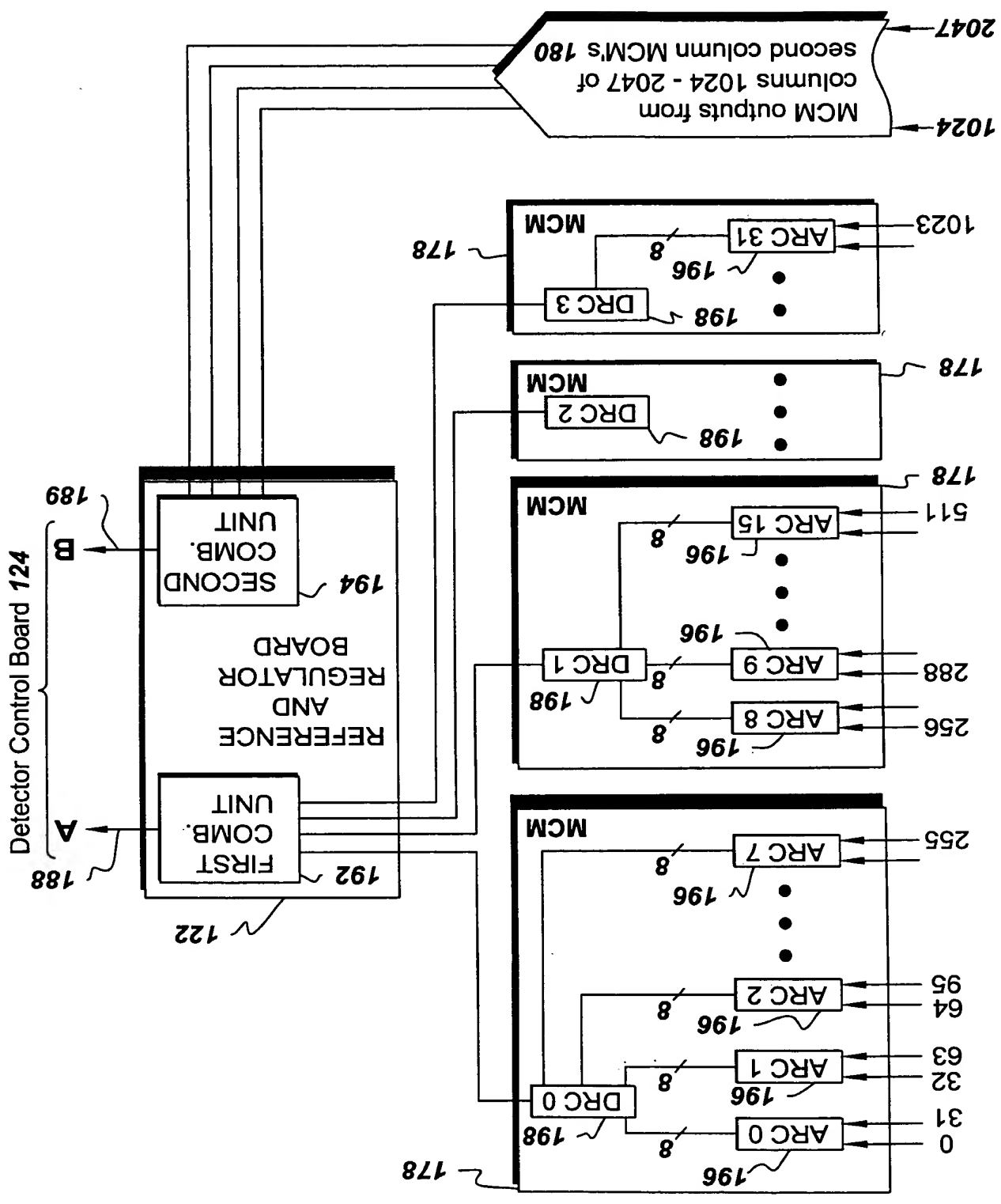
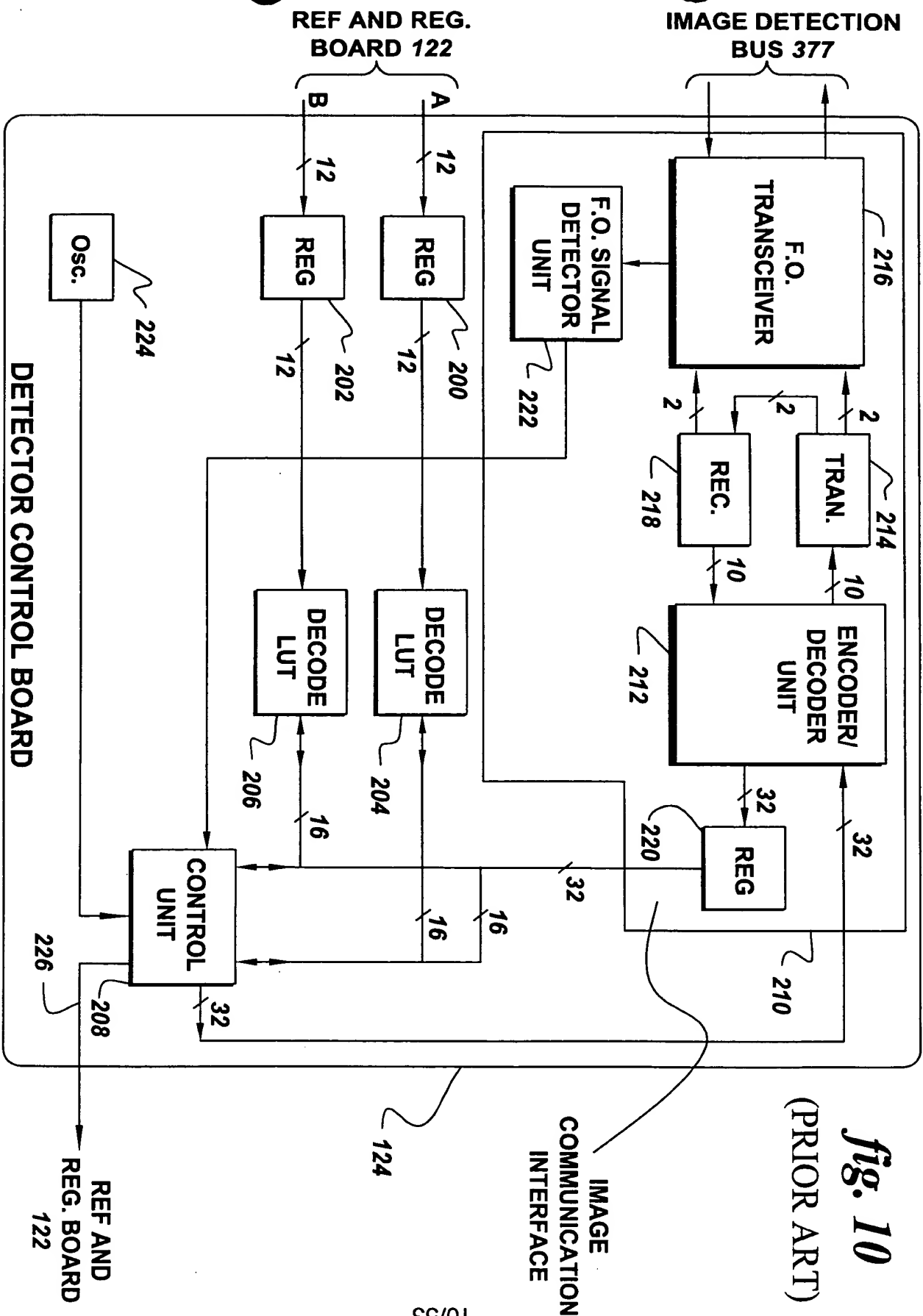
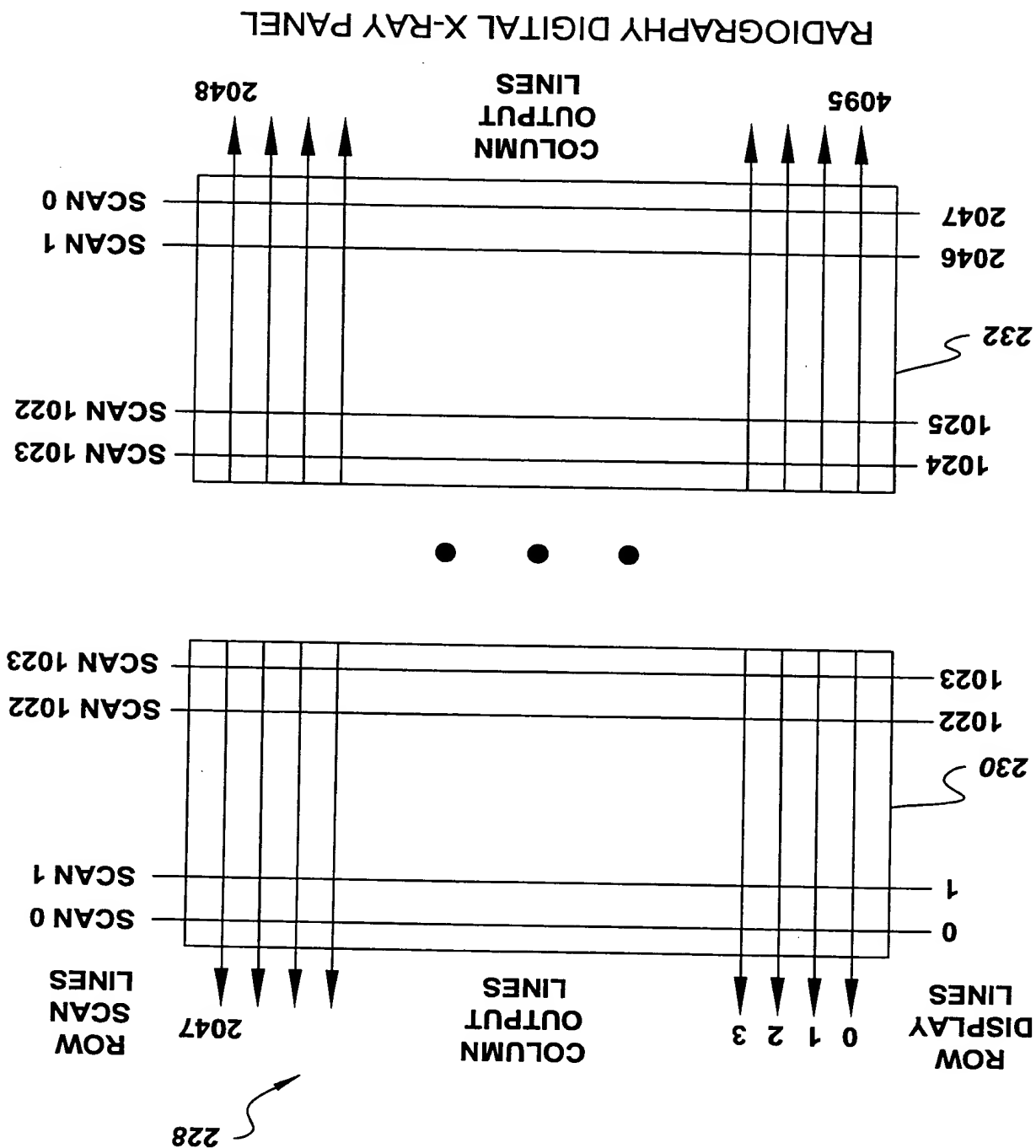


fig. 9 (PRIOR ART)



**fig. 10**  
(PRIOR ART)

fig. 11 (PRIOR ART)



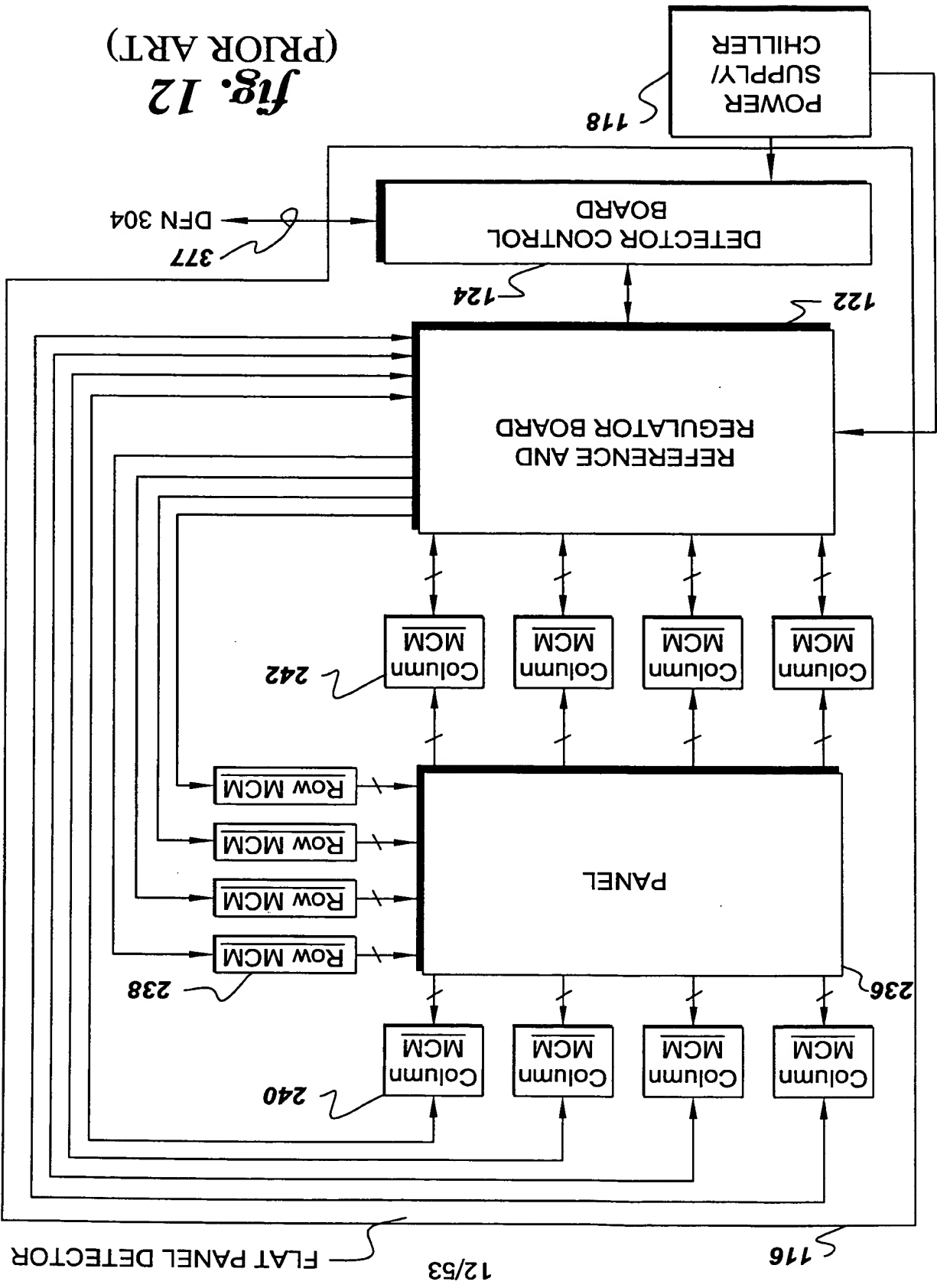
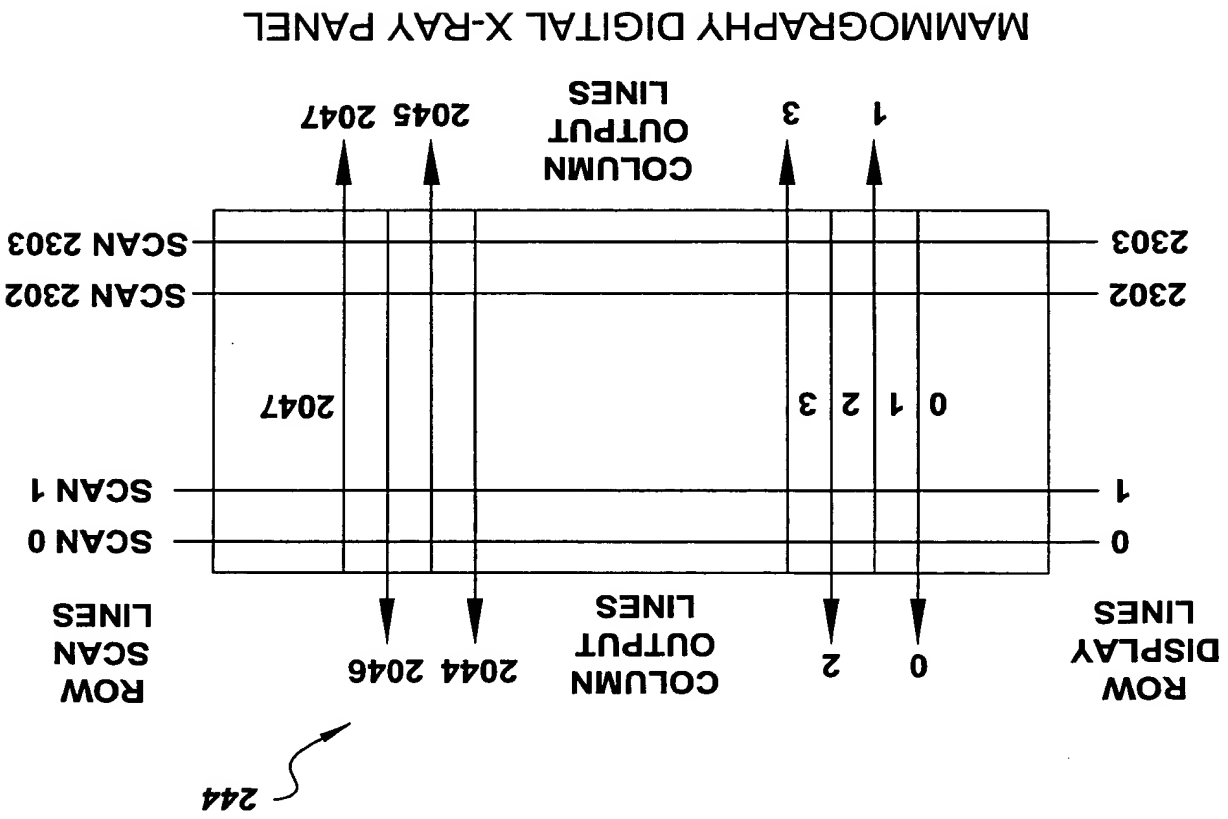


fig. 12  
(PRIOR ART)

*fig. 13*  
(PRIOR ART)



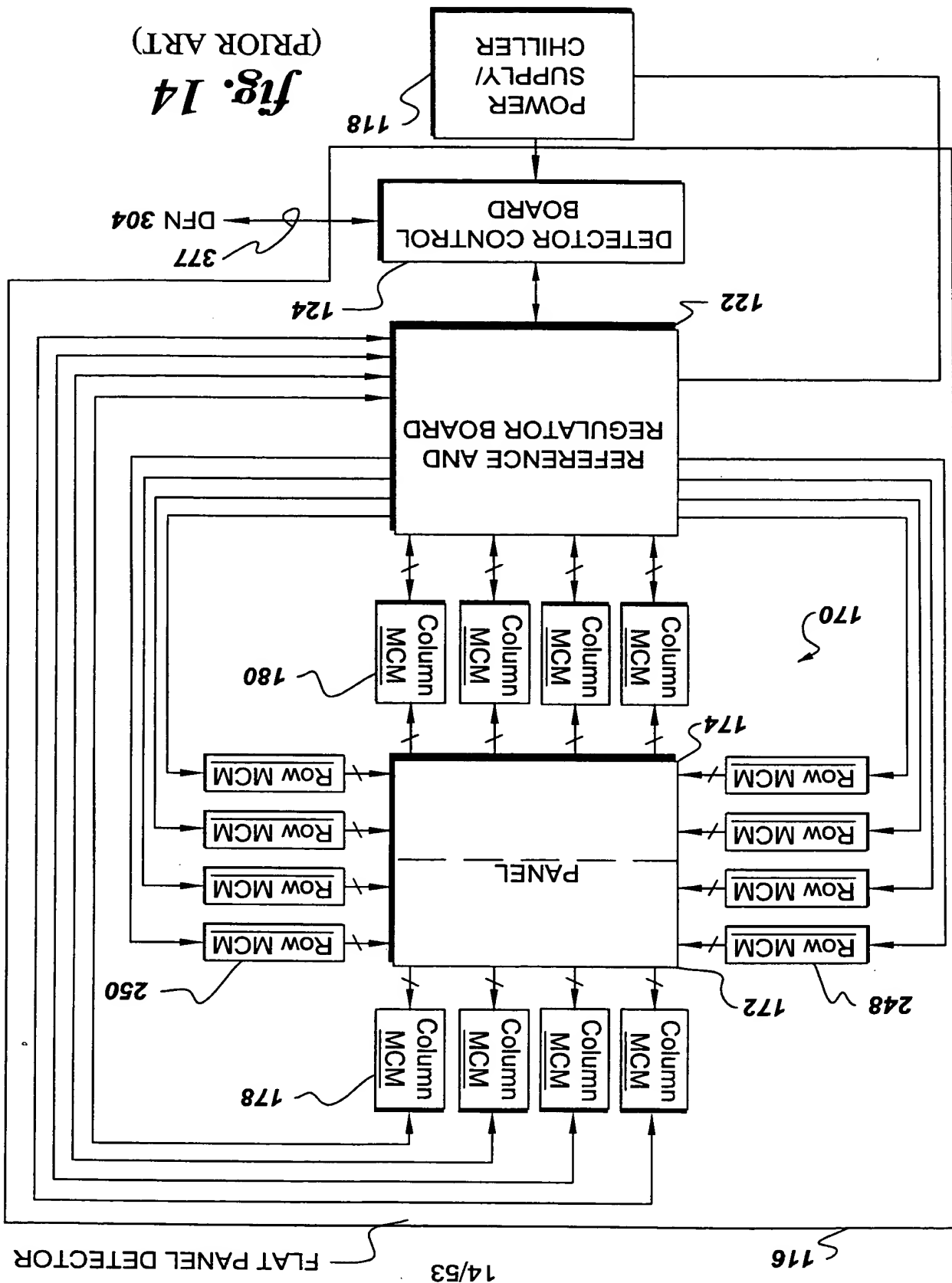
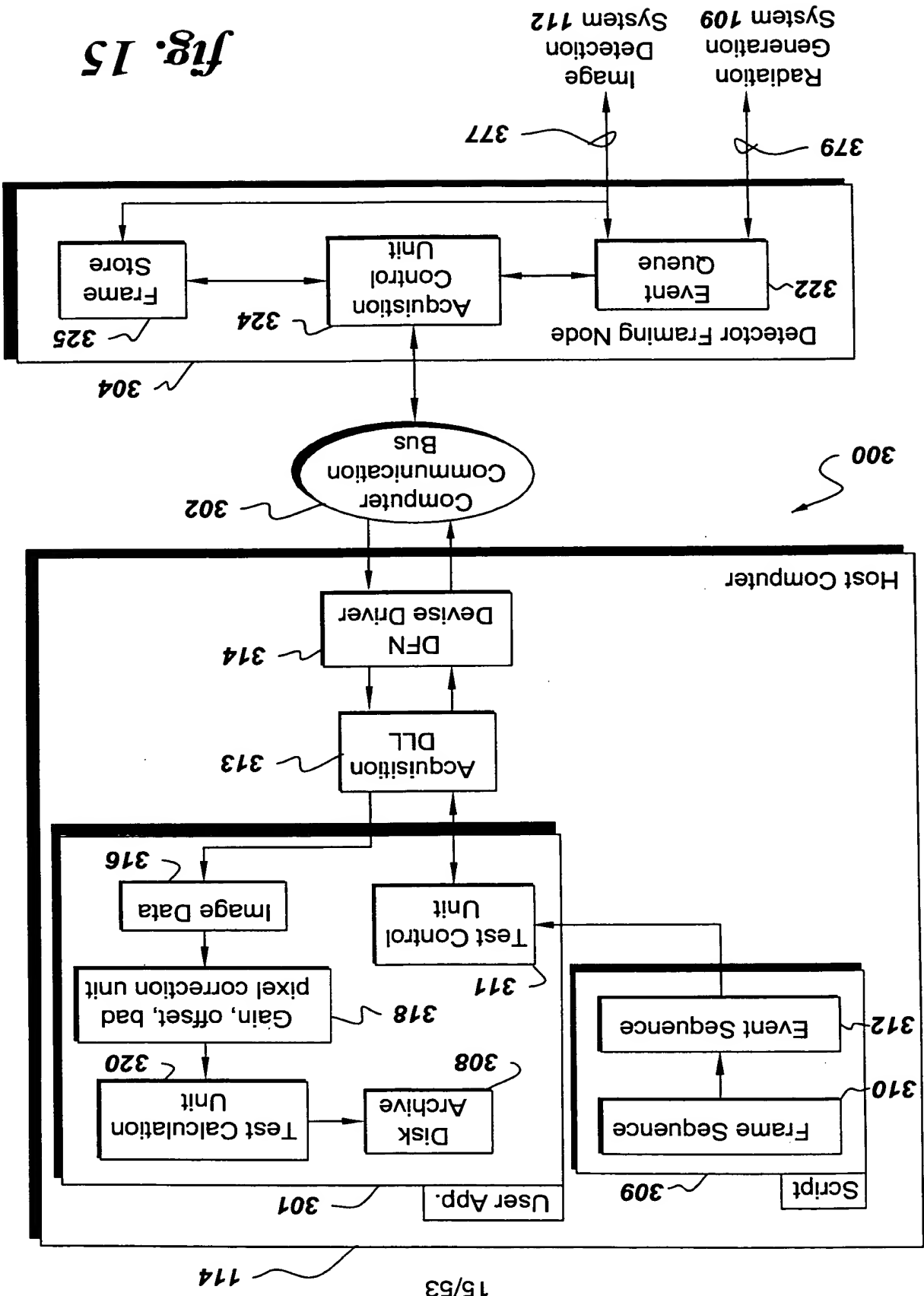
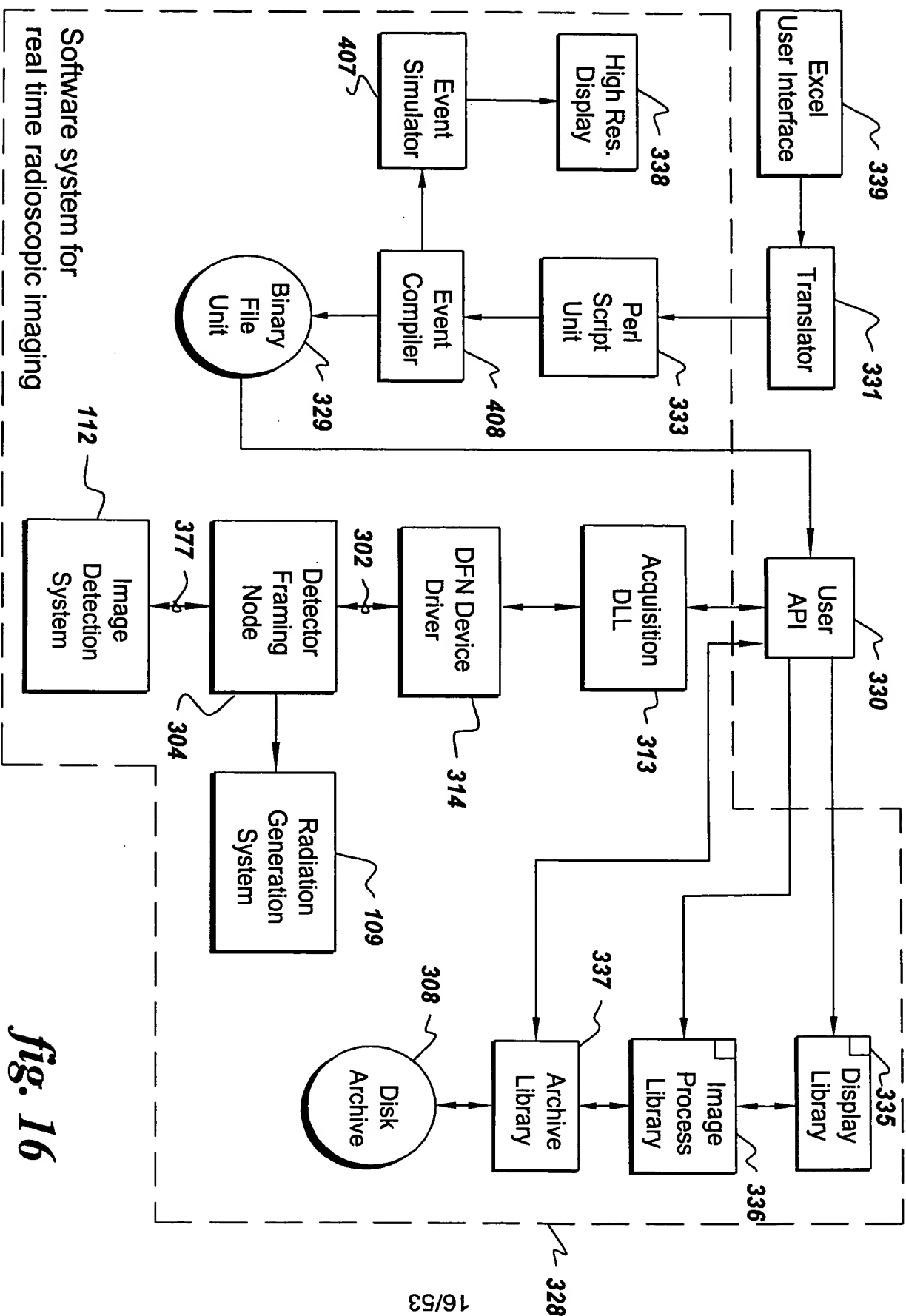


fig. 14  
(PRIOR ART)



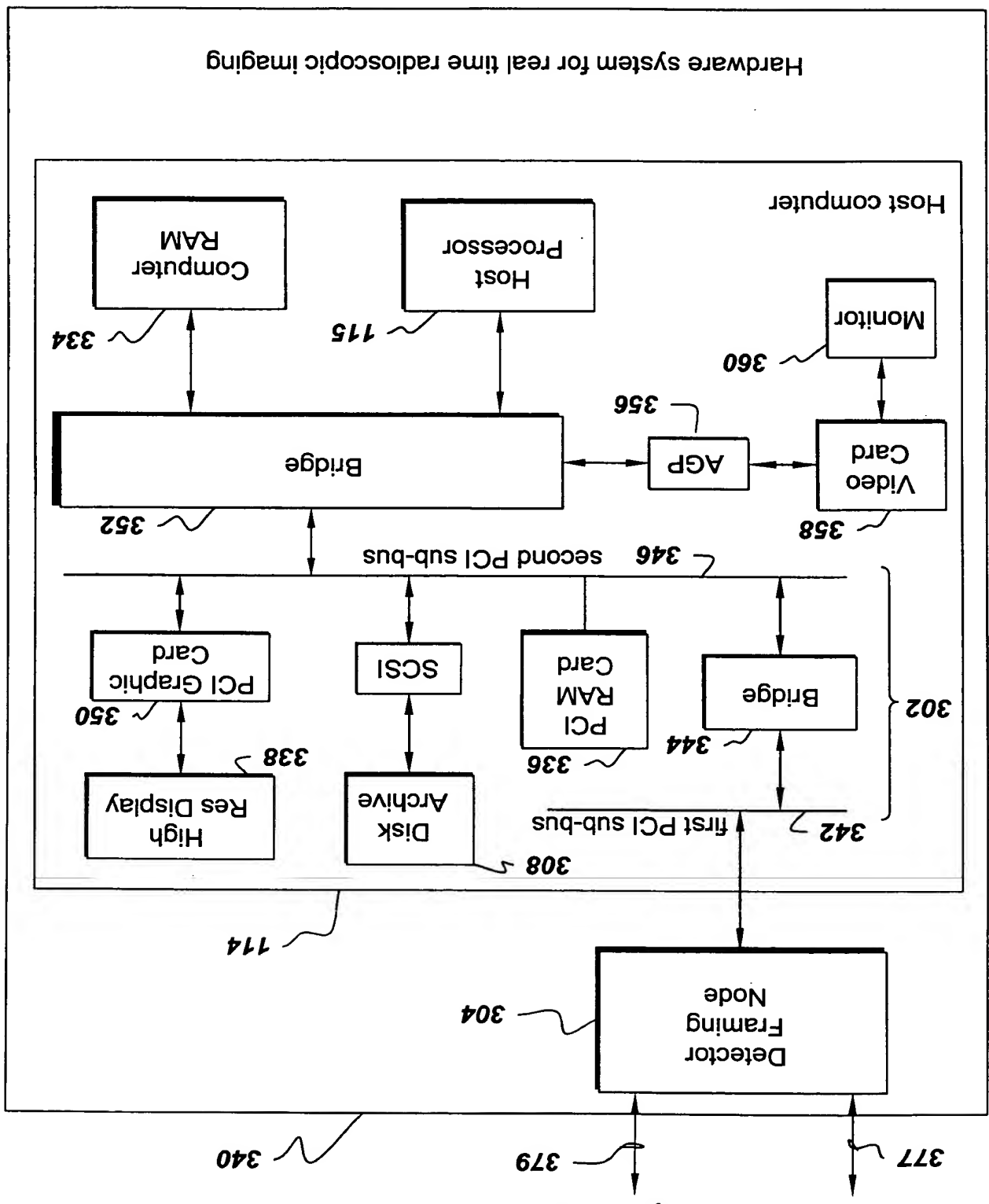




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fig. 17

Image Detection System 112  
Radiation Generation System 109



Hardware system for real time radioscopic imaging

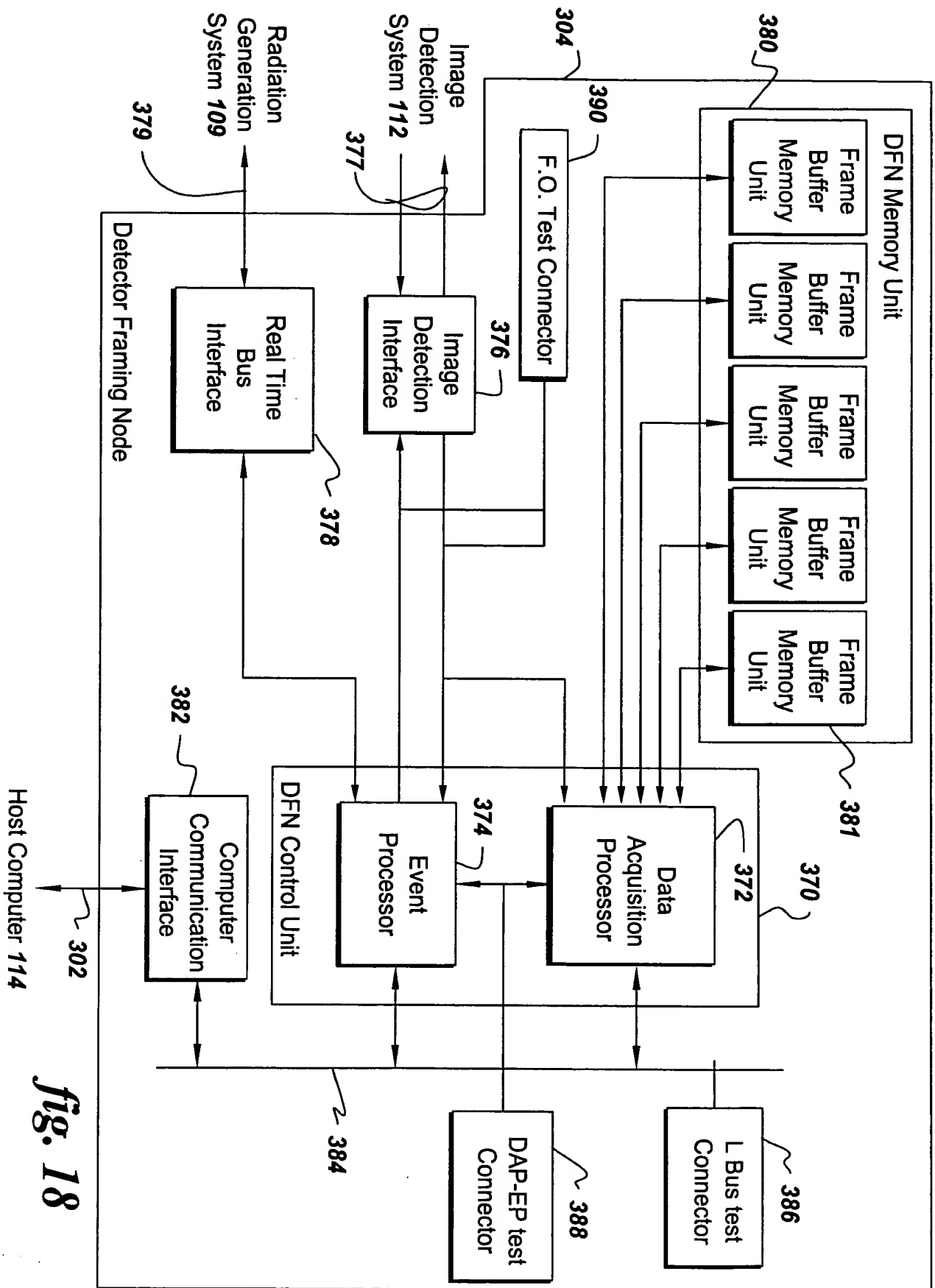


fig. 18

		(fm/sec)	length	latency	memory	offset	gbr
Panel Setup	Real Time	30	unlimited	<5 frames	host	none	
Single Frame	Post Process	-	-	Delay ~.1 sec	"	y	
Single Frame	Post Process	-	-	Delay ~.2 sec	"	y	y
Real Time	Real Time	R	unlimited	<5 frames	host	none	
Real Time	Real Time	R-X	unlimited	<5 frames	"	y	
Real Time	Real Time	R-Y	unlimited	<5 frames	"	y	y

fig. 19

Modality	image size	Frames Stored
		host memory
Cardiac	1024 X 1024	200
Rad	2048 X 2048	50
Mammo	2304 X 2048	44

fig. 20

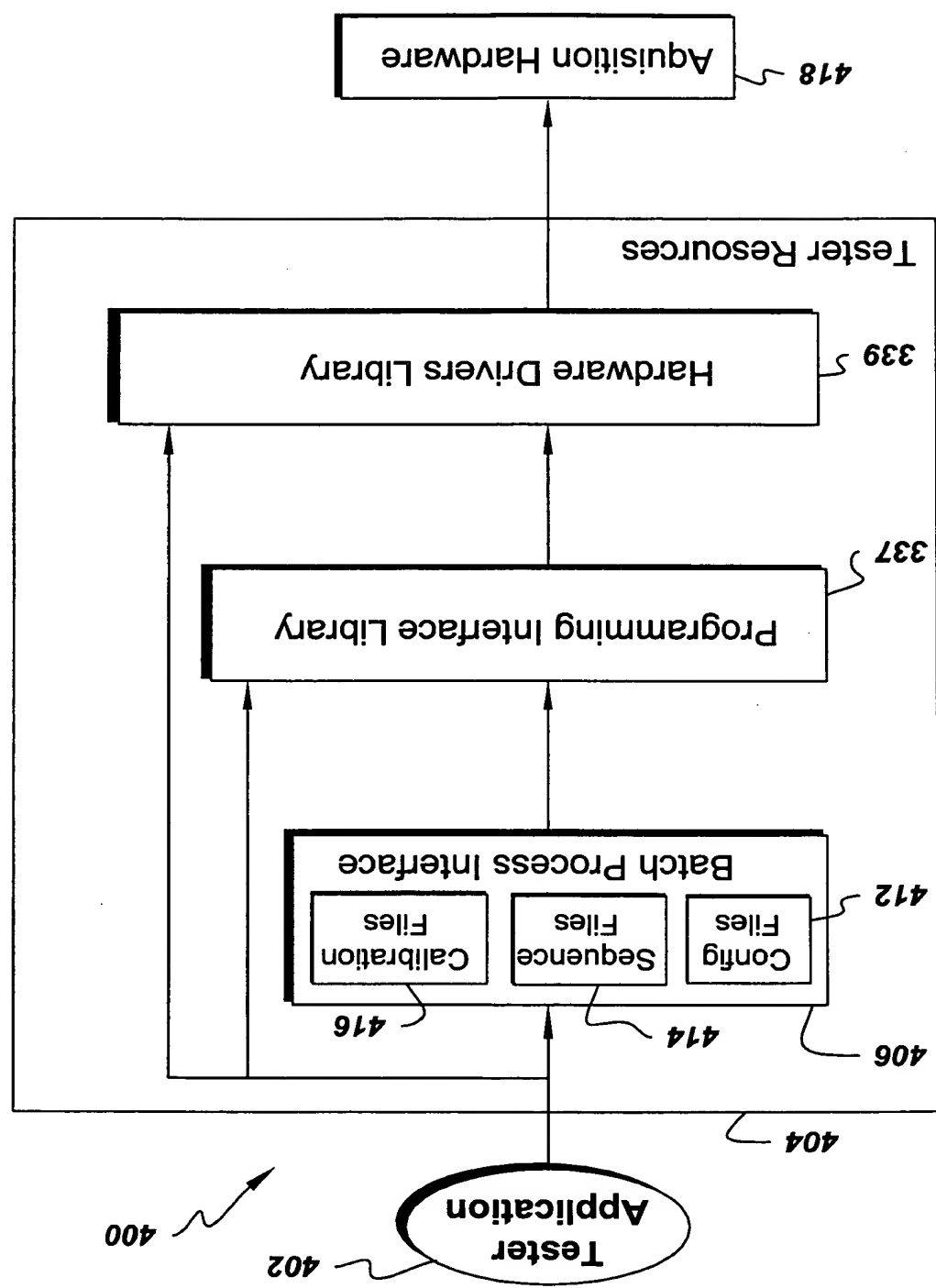


fig. 21

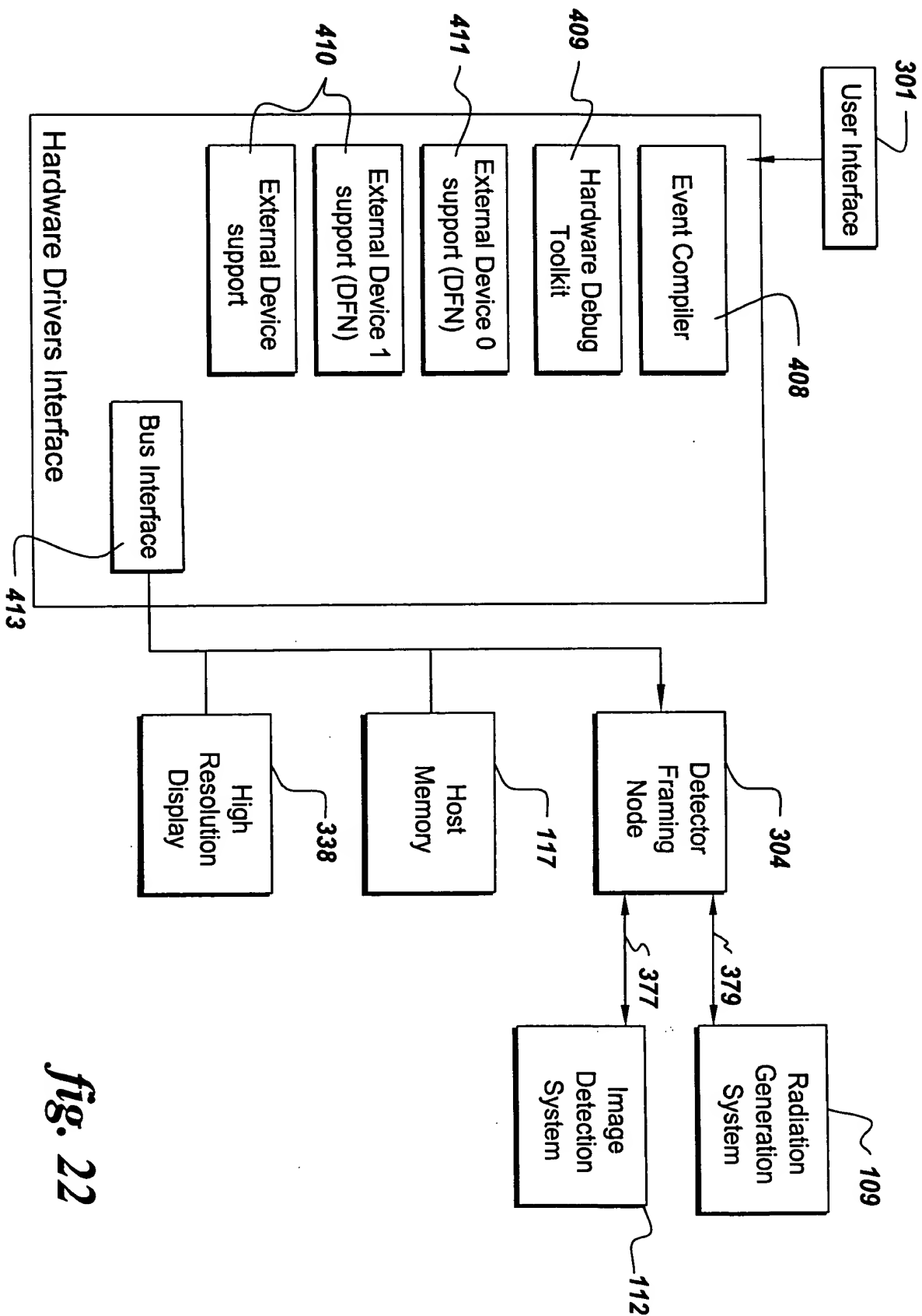
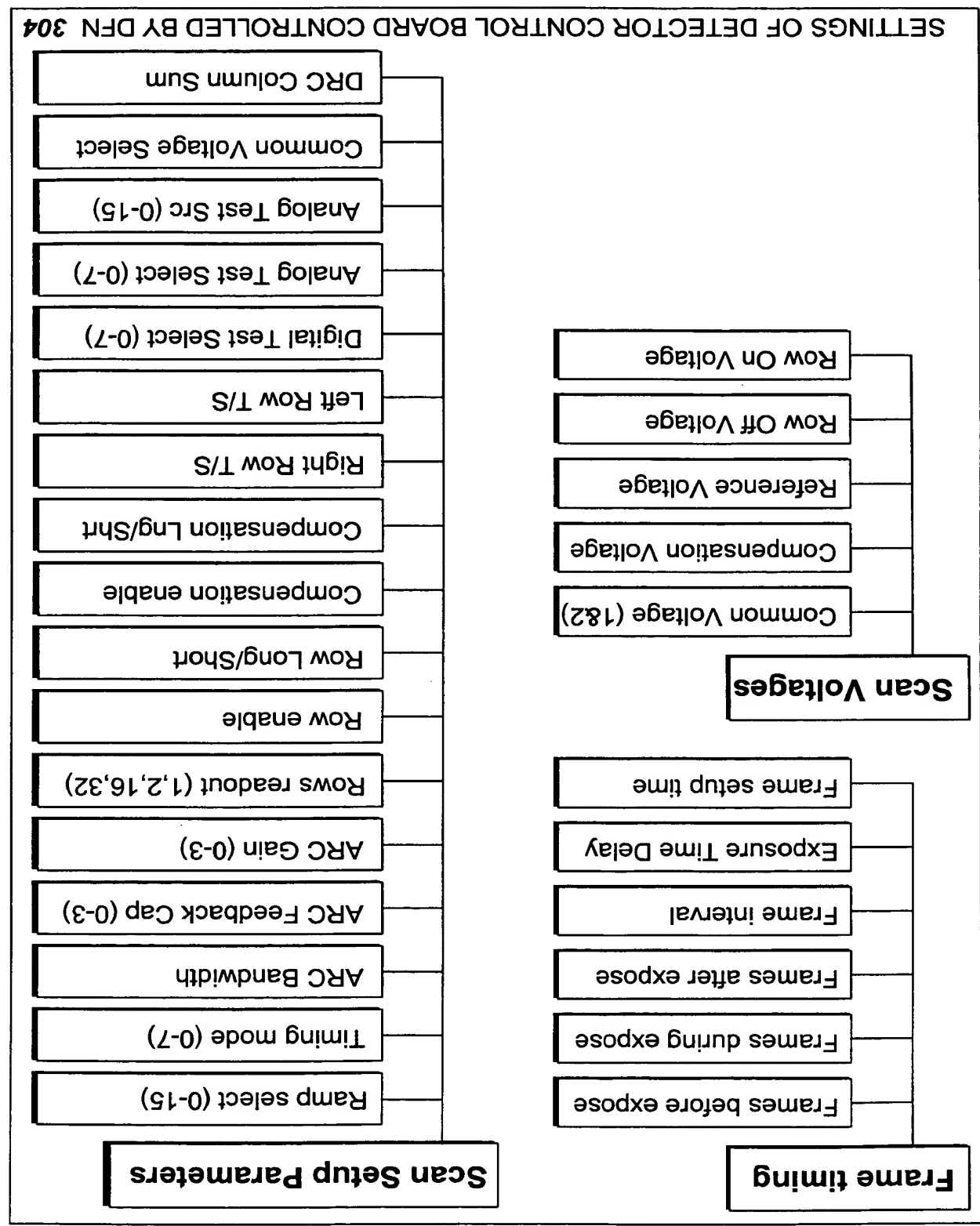


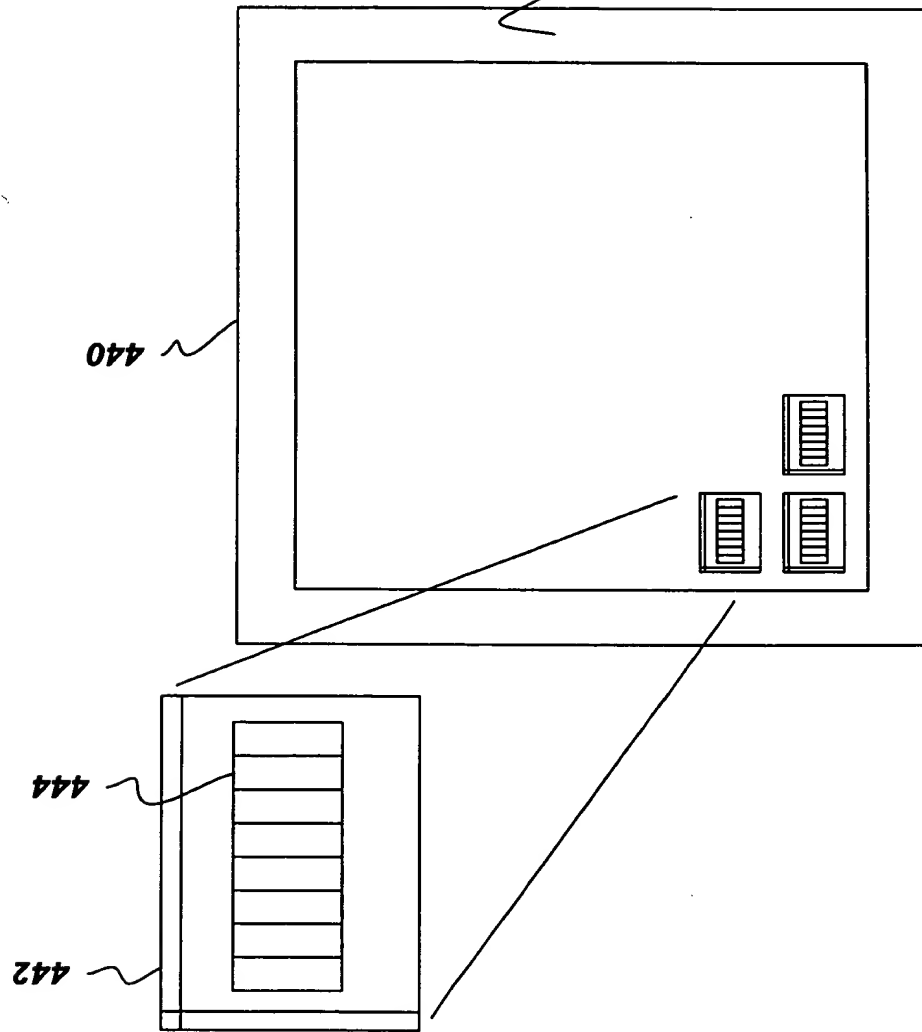
fig. 22

fig. 23



**fig. 24**

FIELD PROGRAMMABLE GATE ARRAY





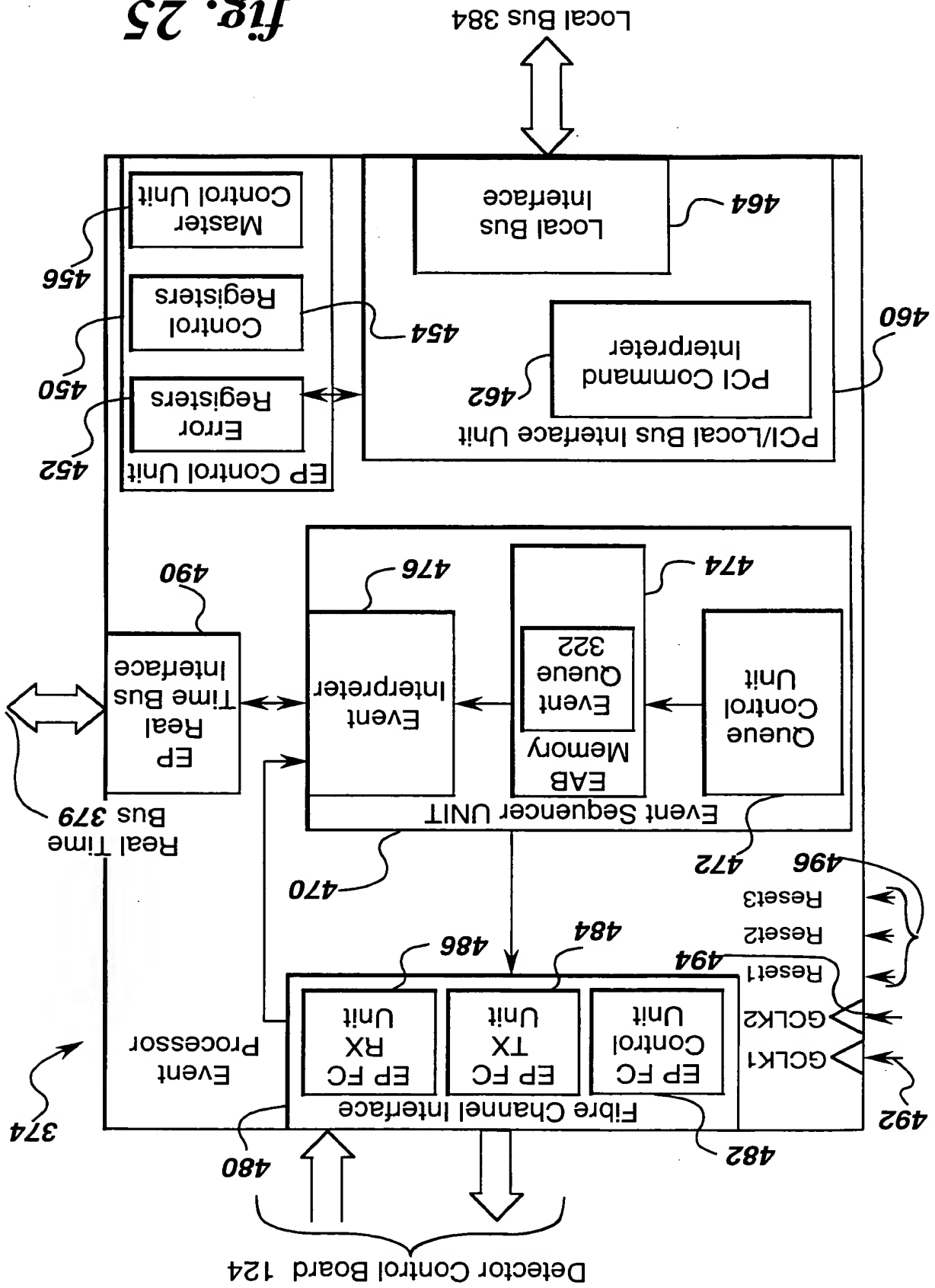
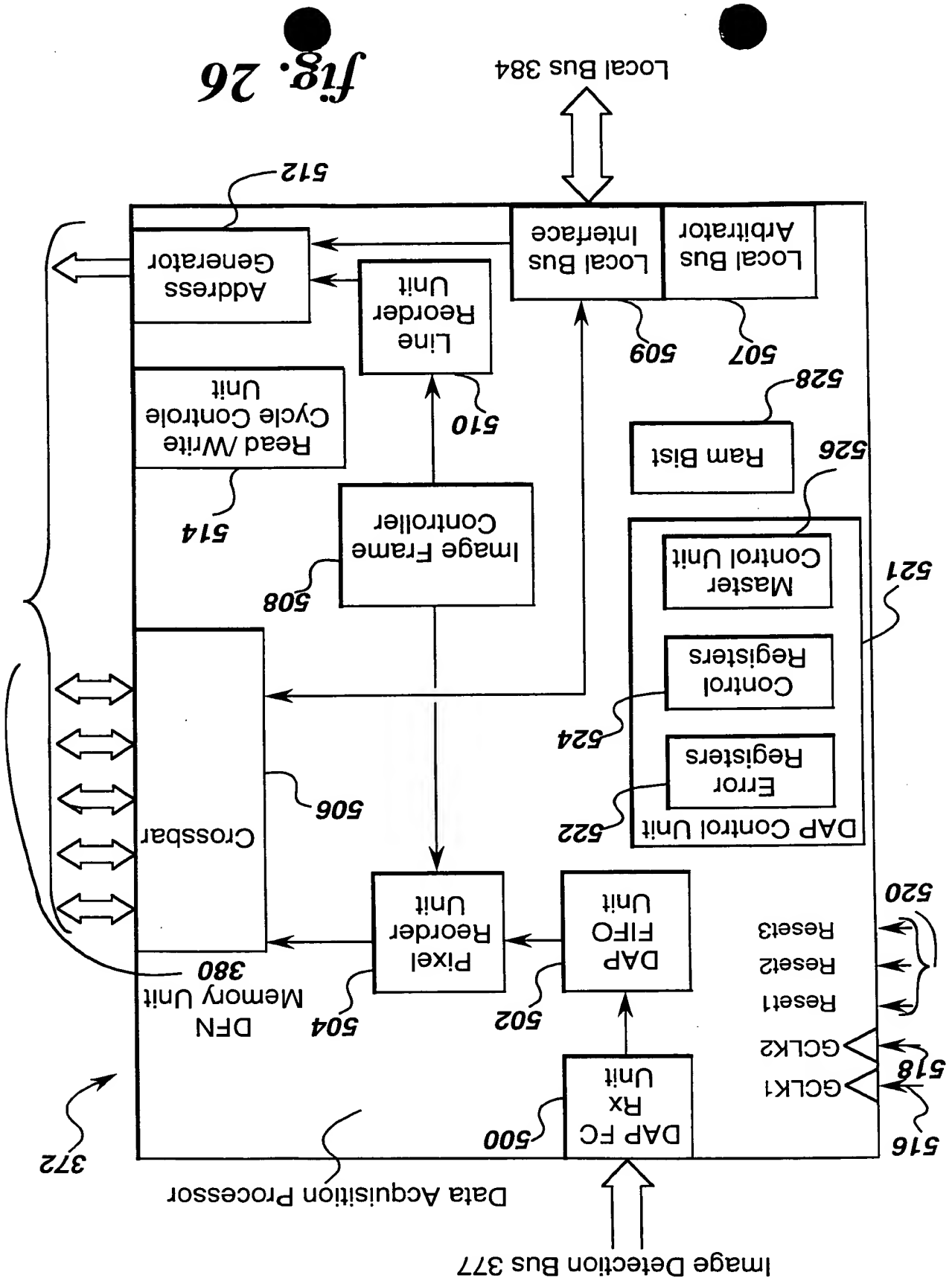


fig. 25

FIG. 26



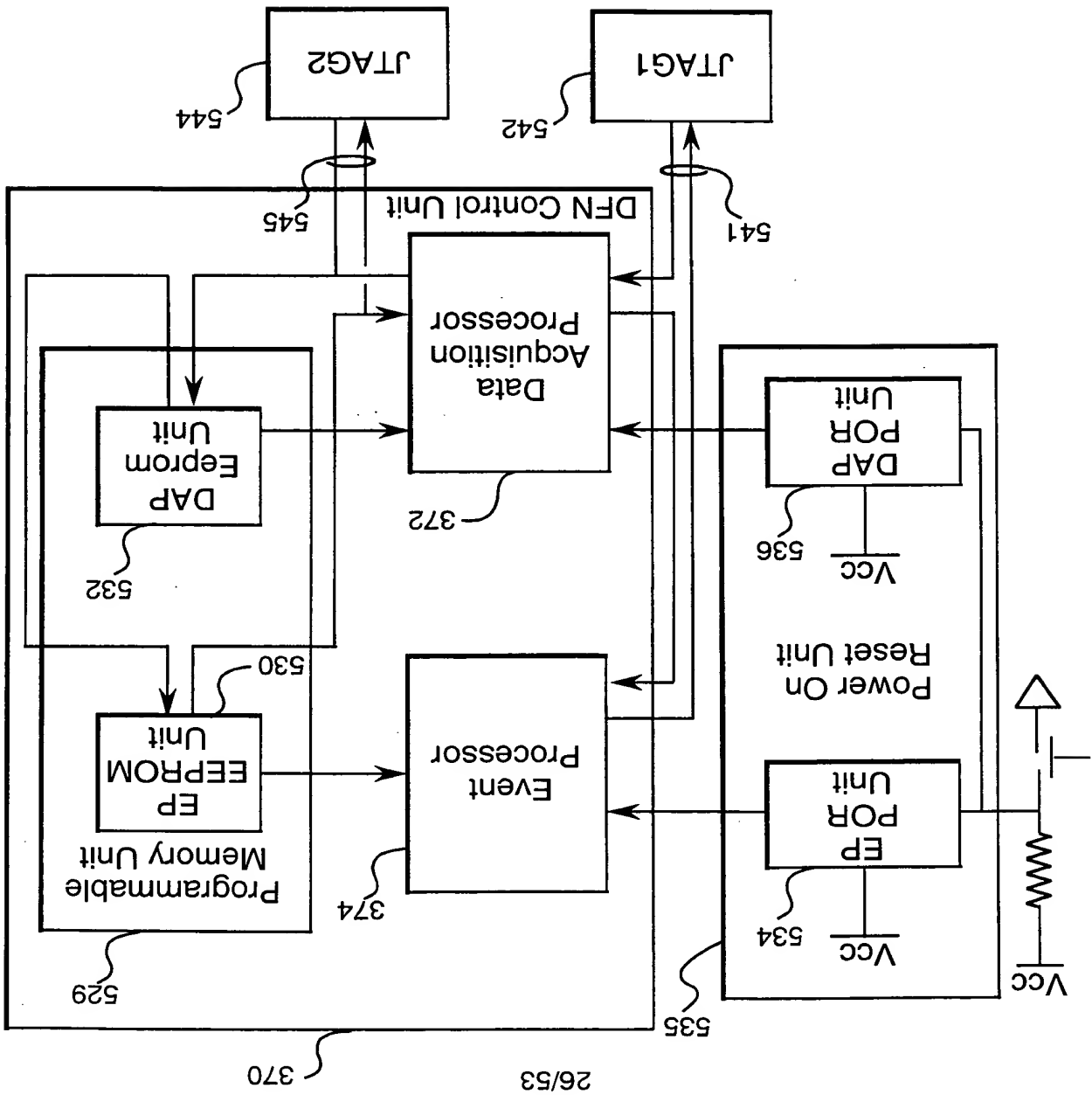


fig. 27

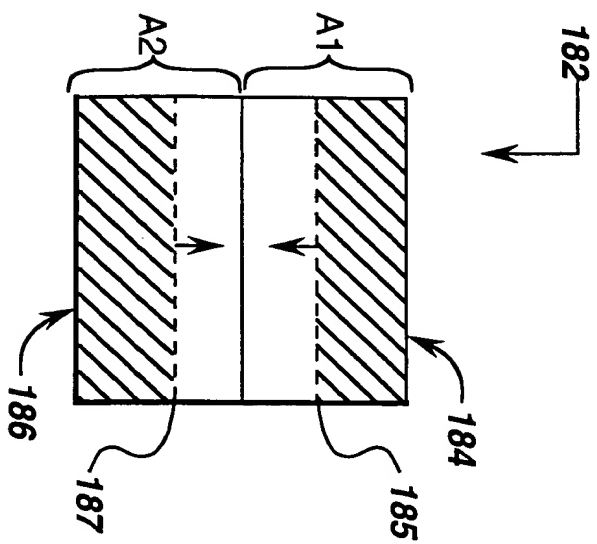


fig. 28

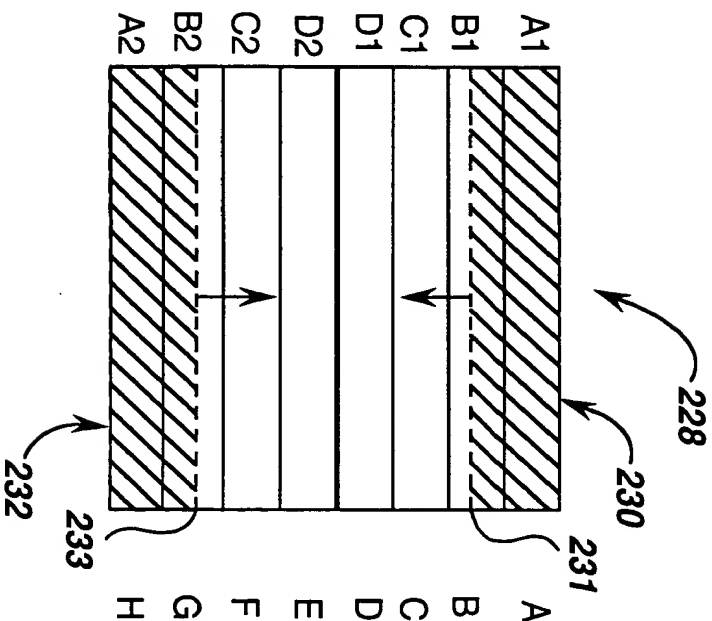


fig. 29

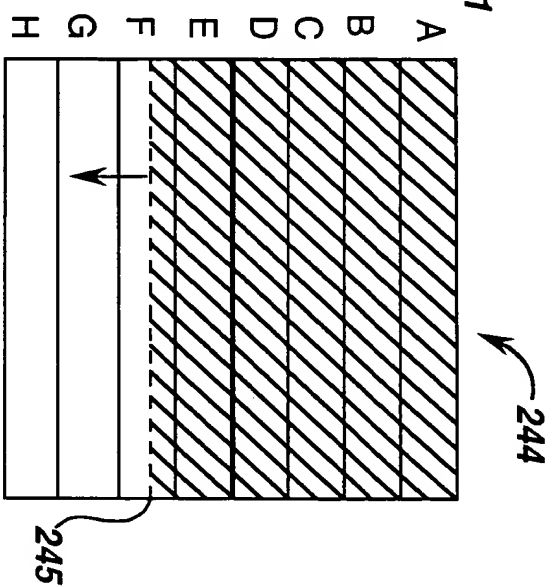


fig. 30

fig. 33

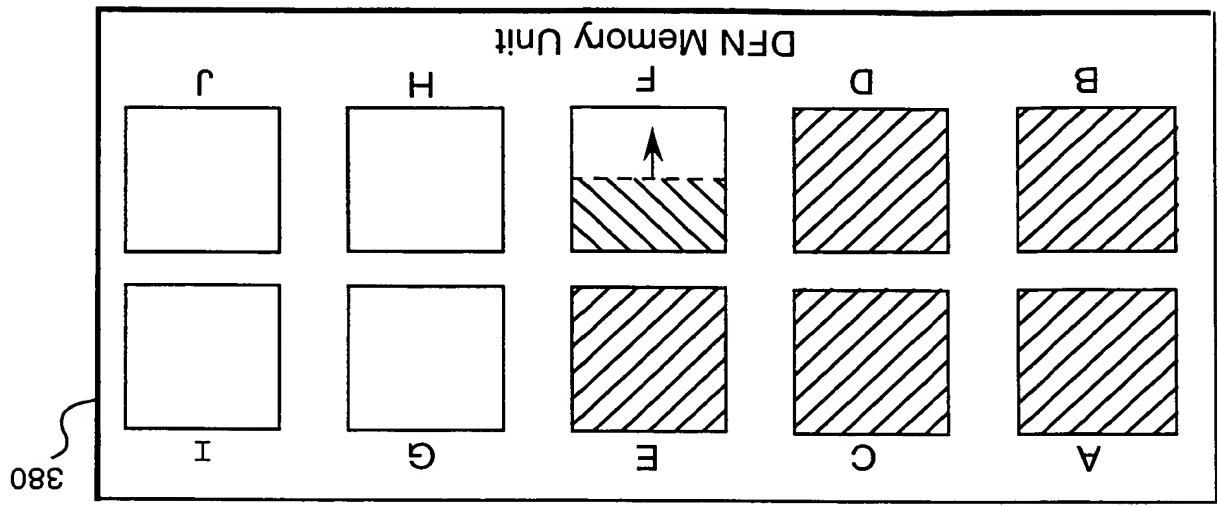


fig. 32

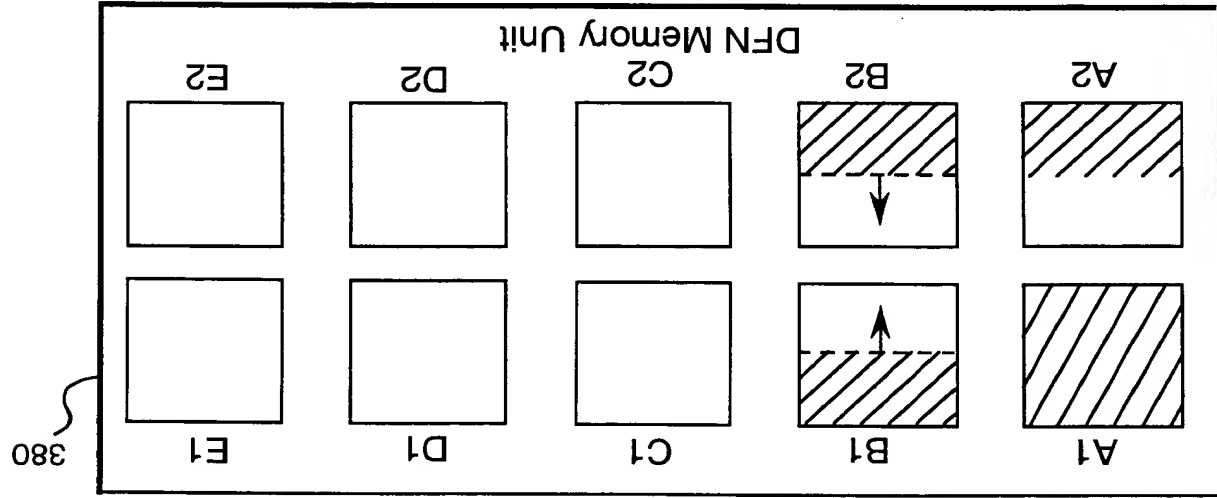
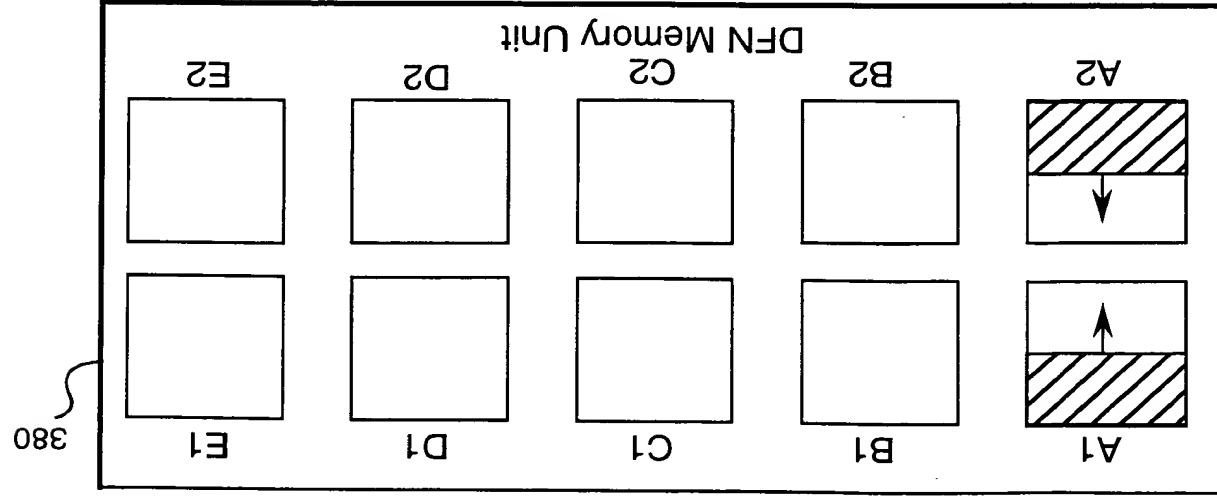


fig. 31



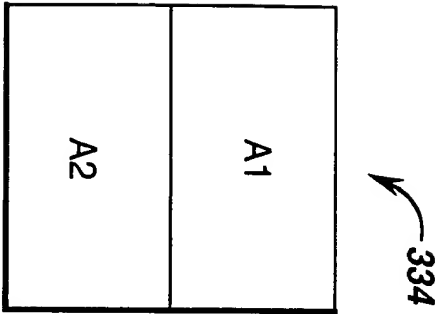


fig. 34

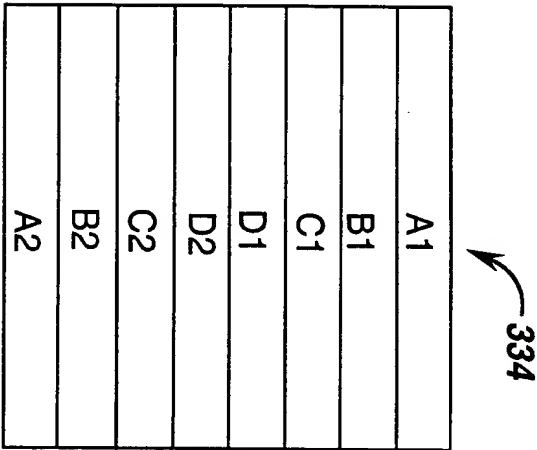


fig. 35

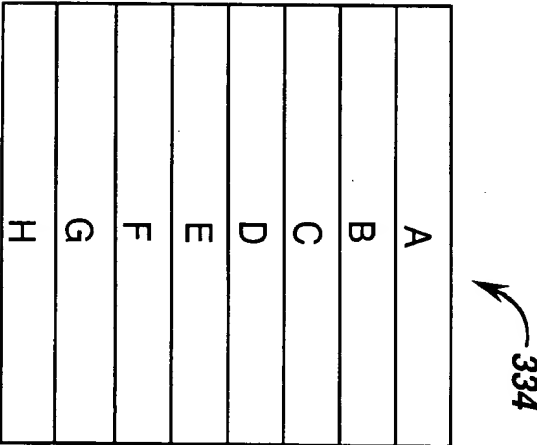


fig. 36

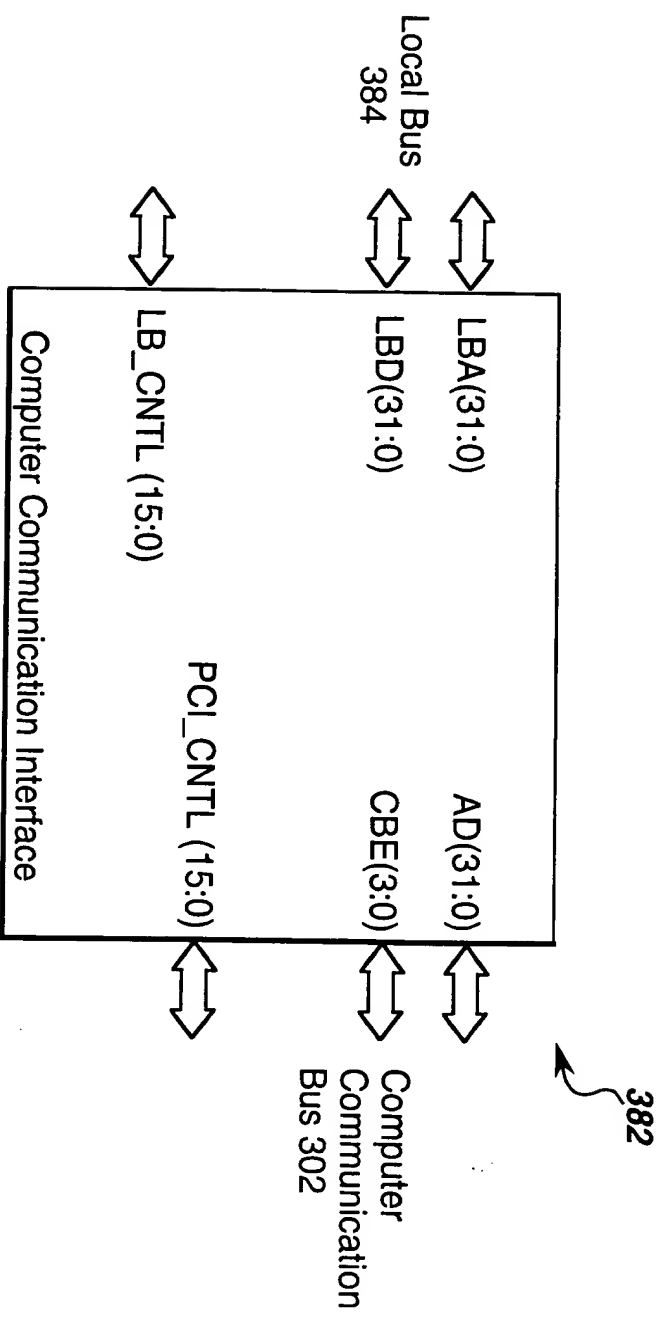


fig. 37

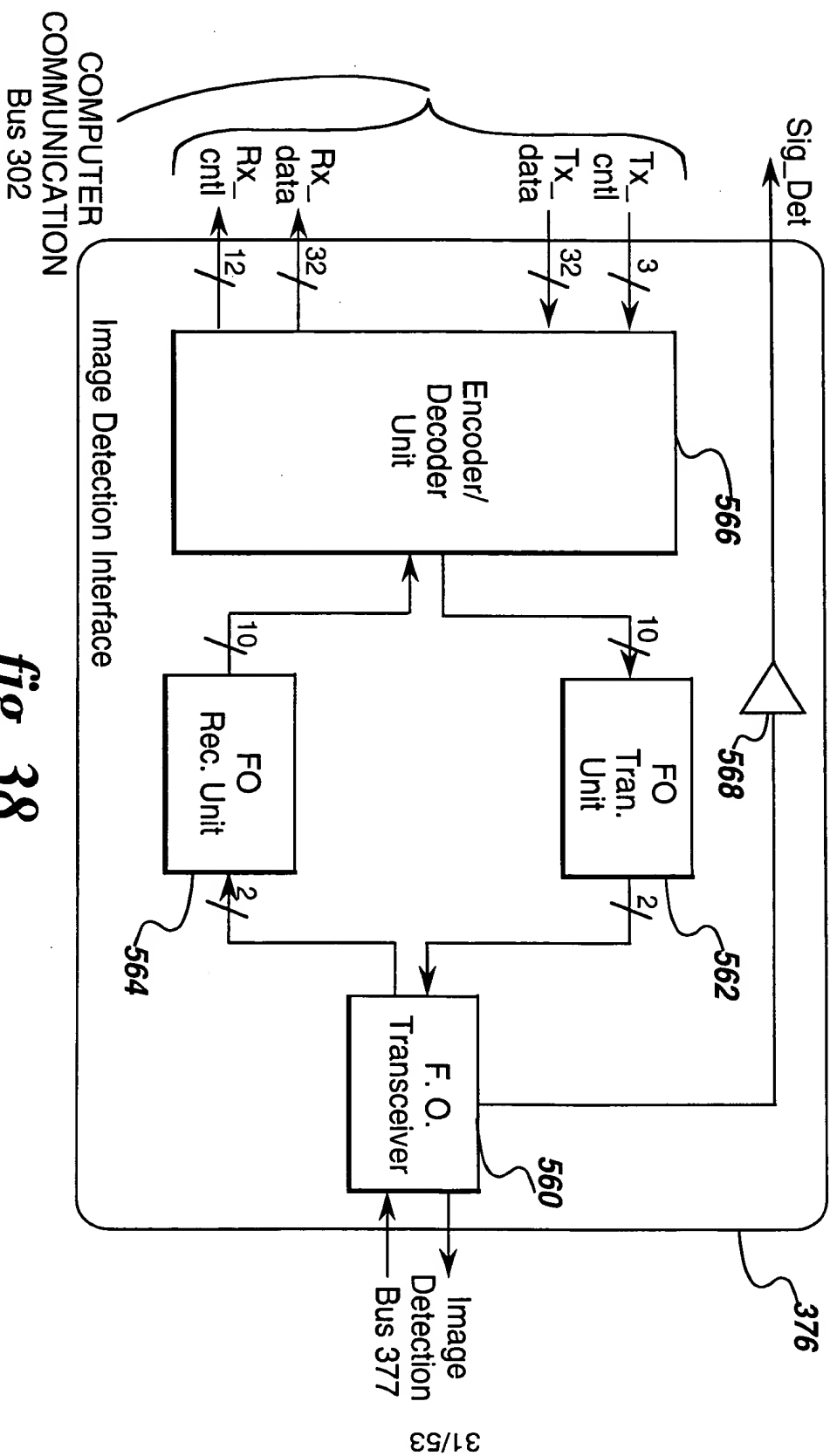


fig. 38



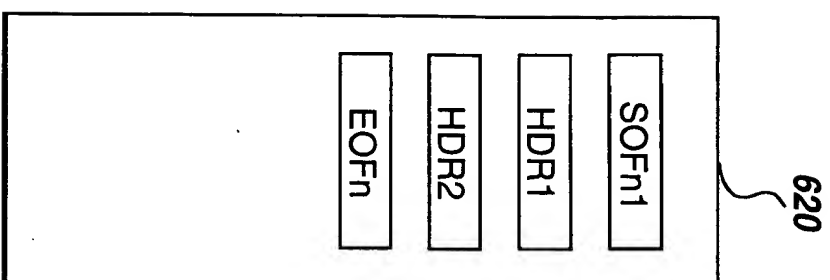


fig. 39

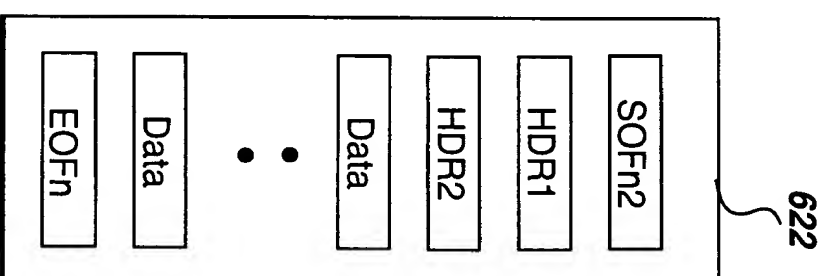


fig. 40

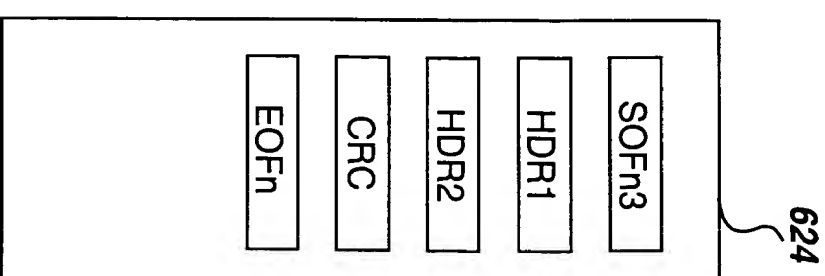


fig. 41

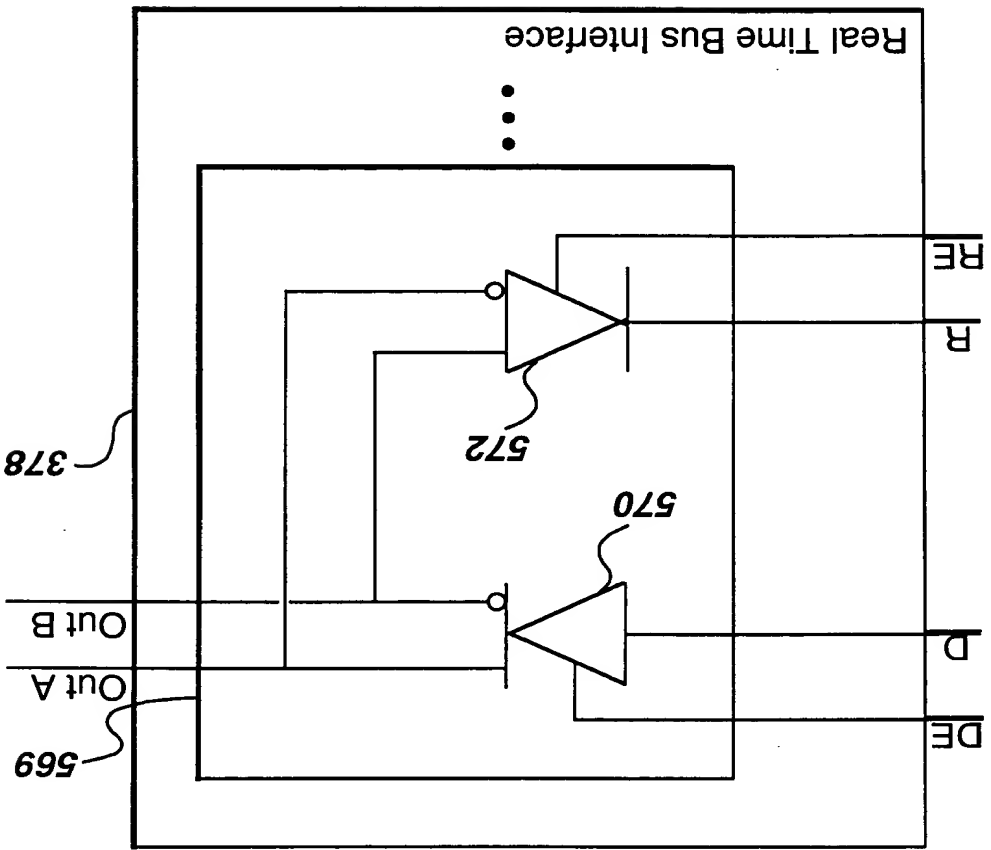


fig. 42

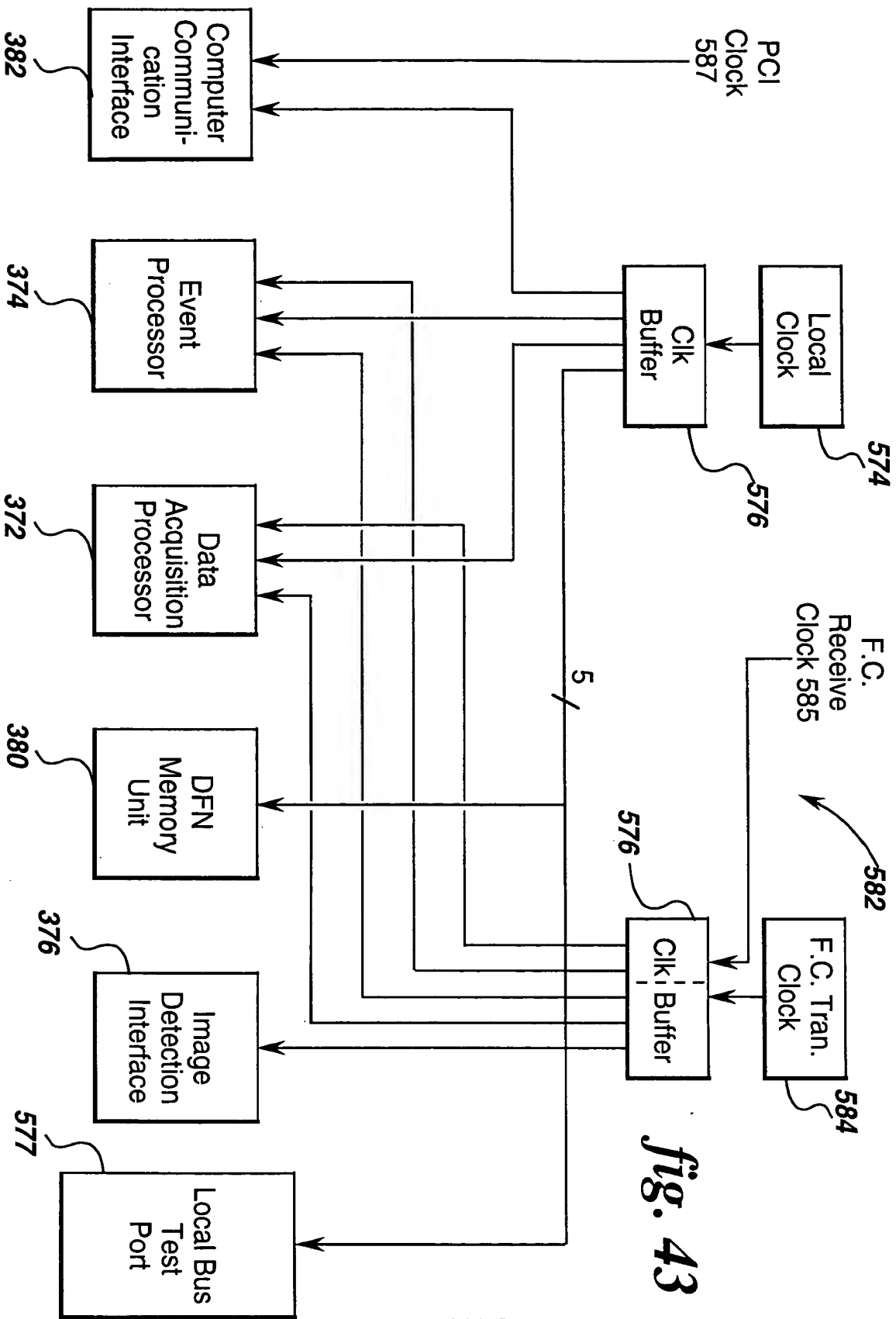
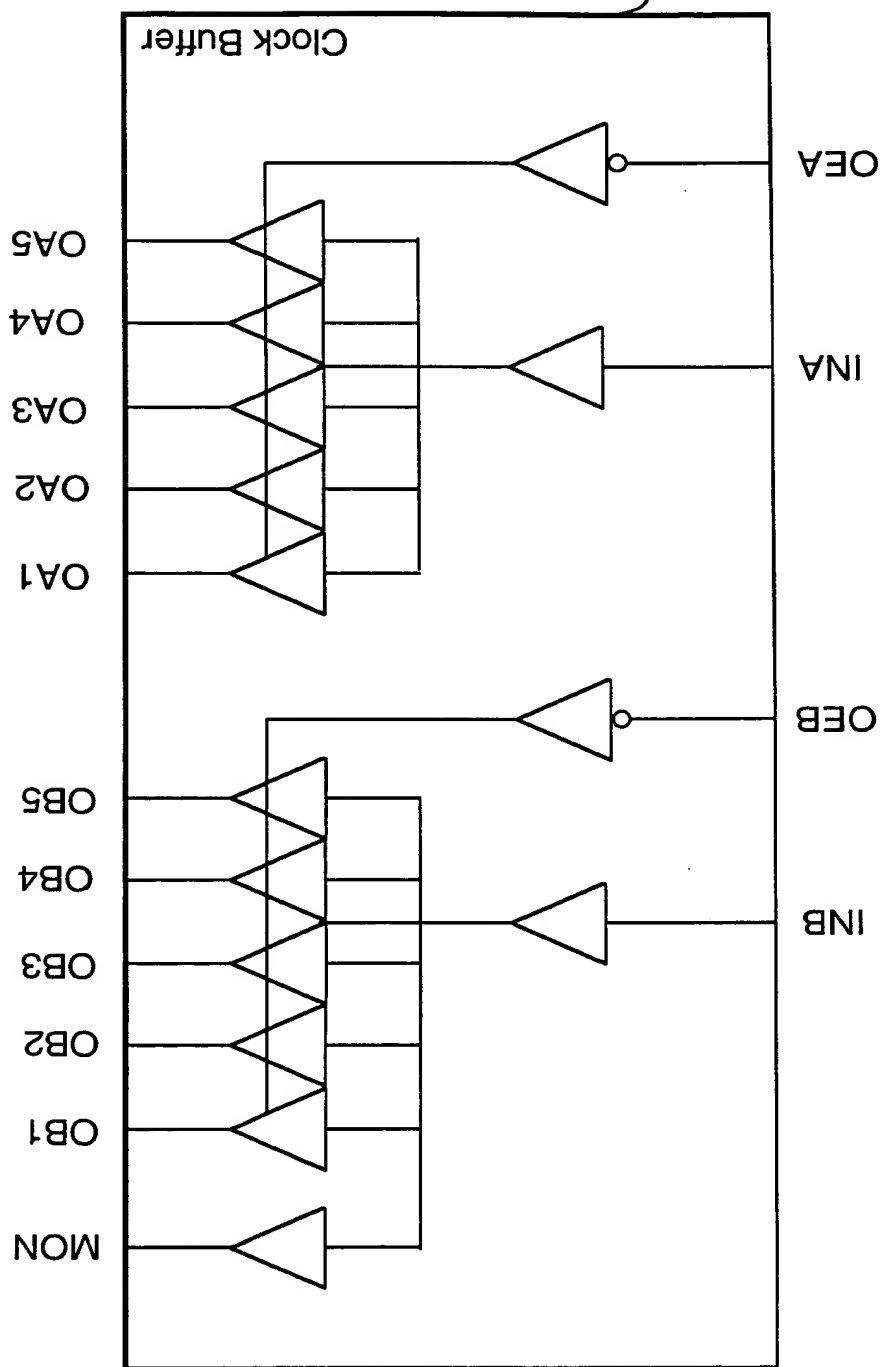


fig. 43



*fig. 44*

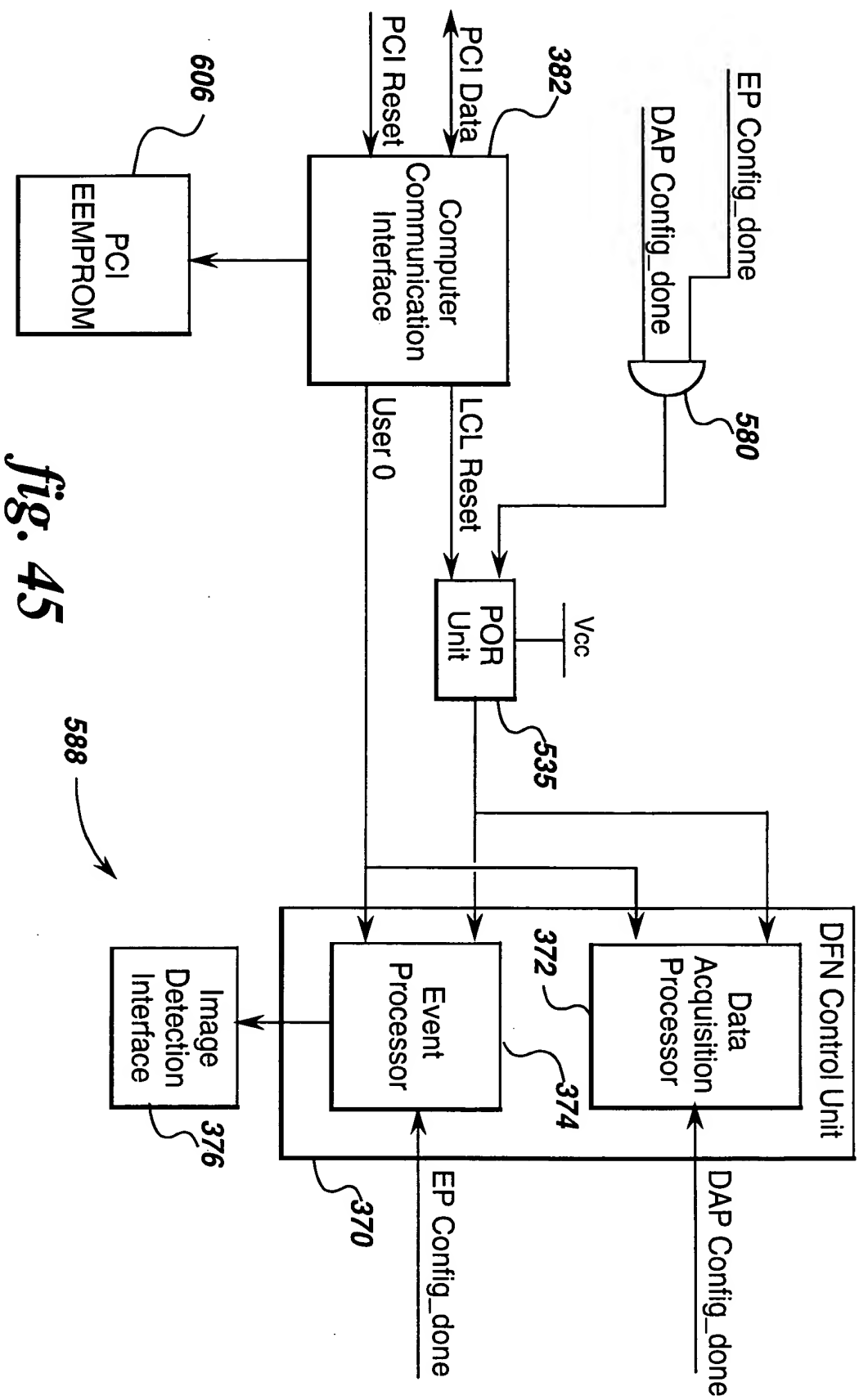


fig. 45

588

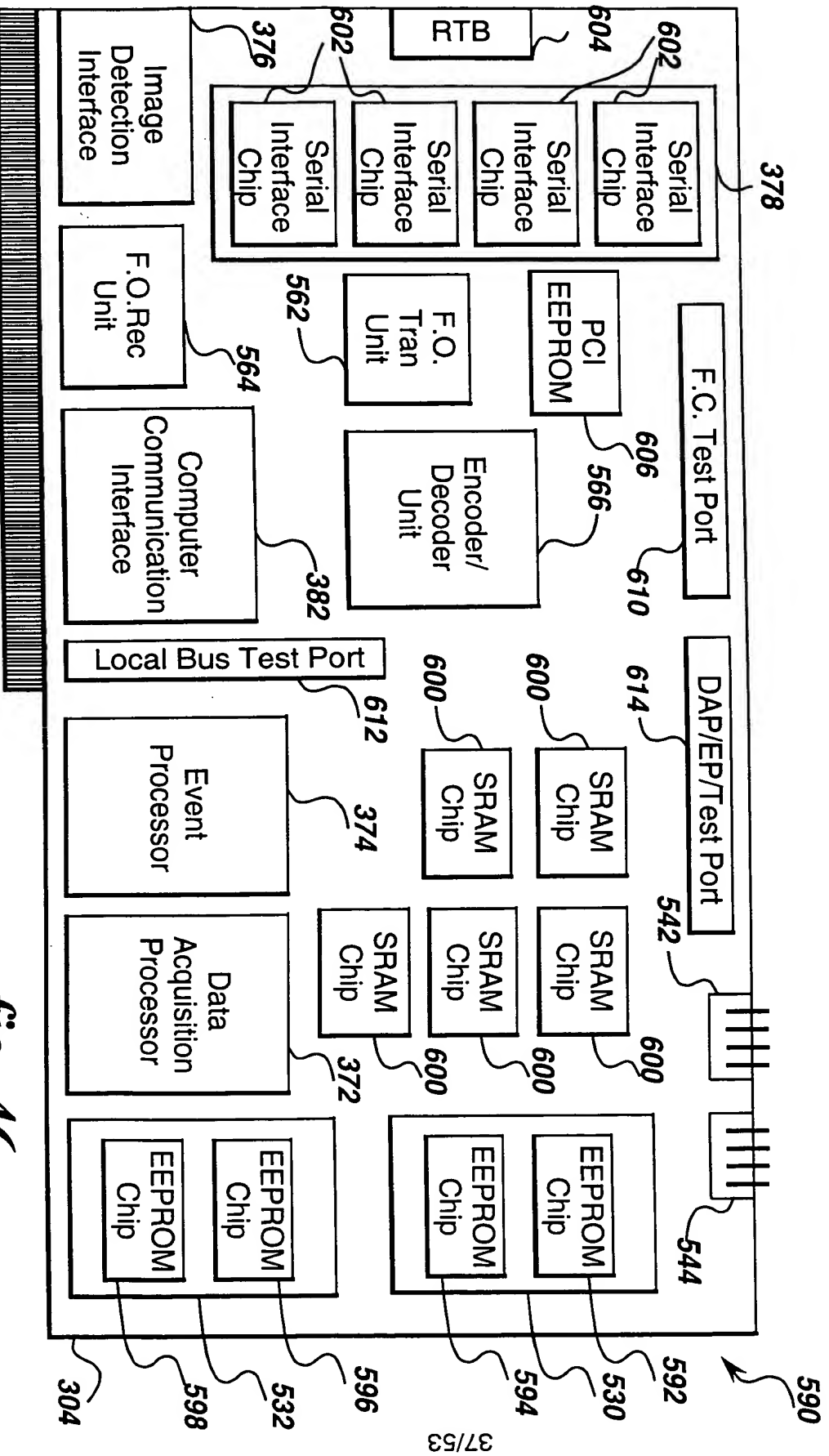
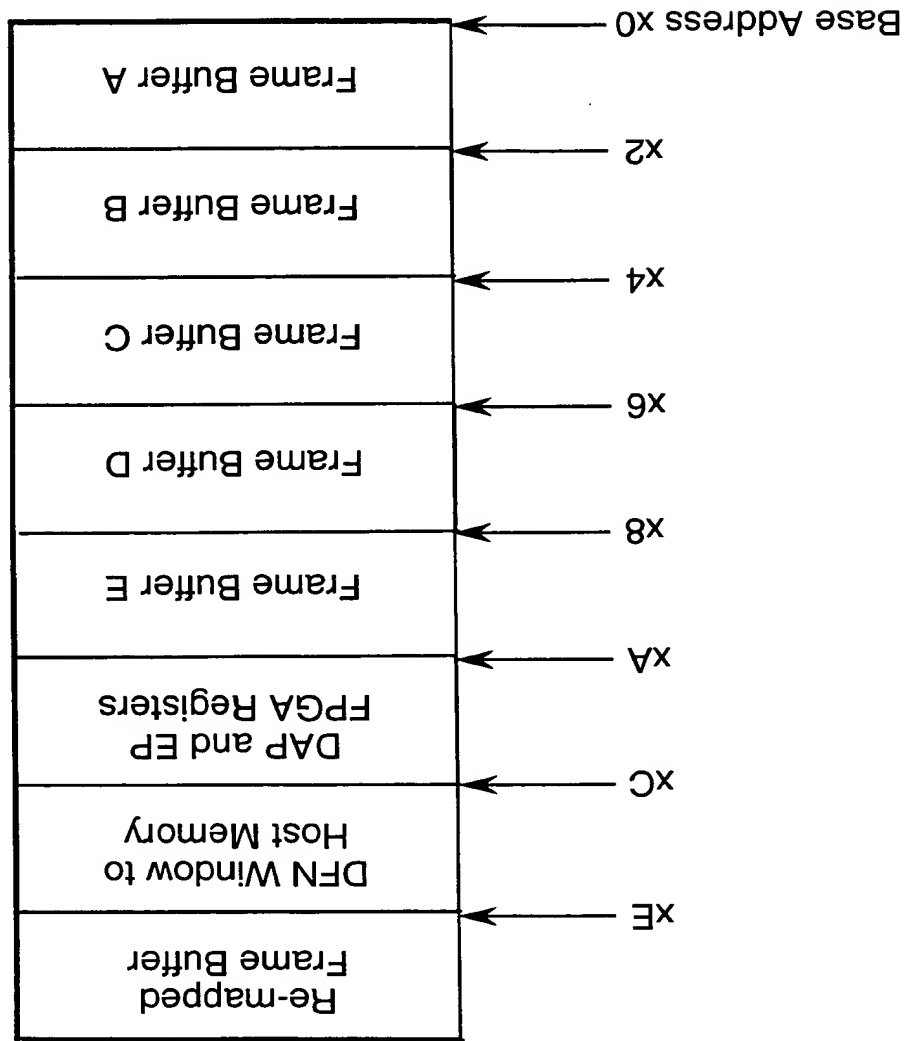


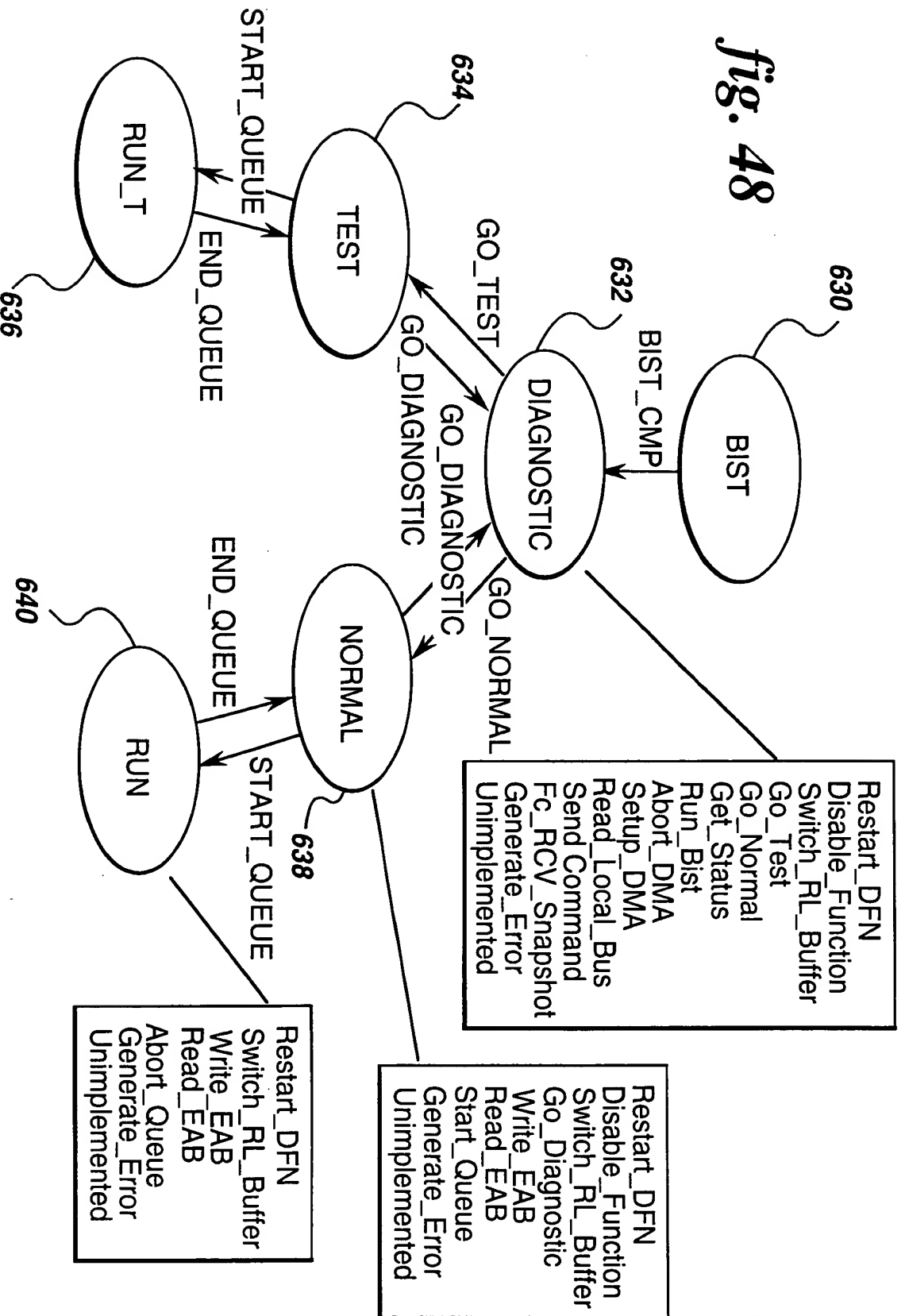
fig. 46

616



Mapping of 16 MByte PCI Address Space

fig. 47





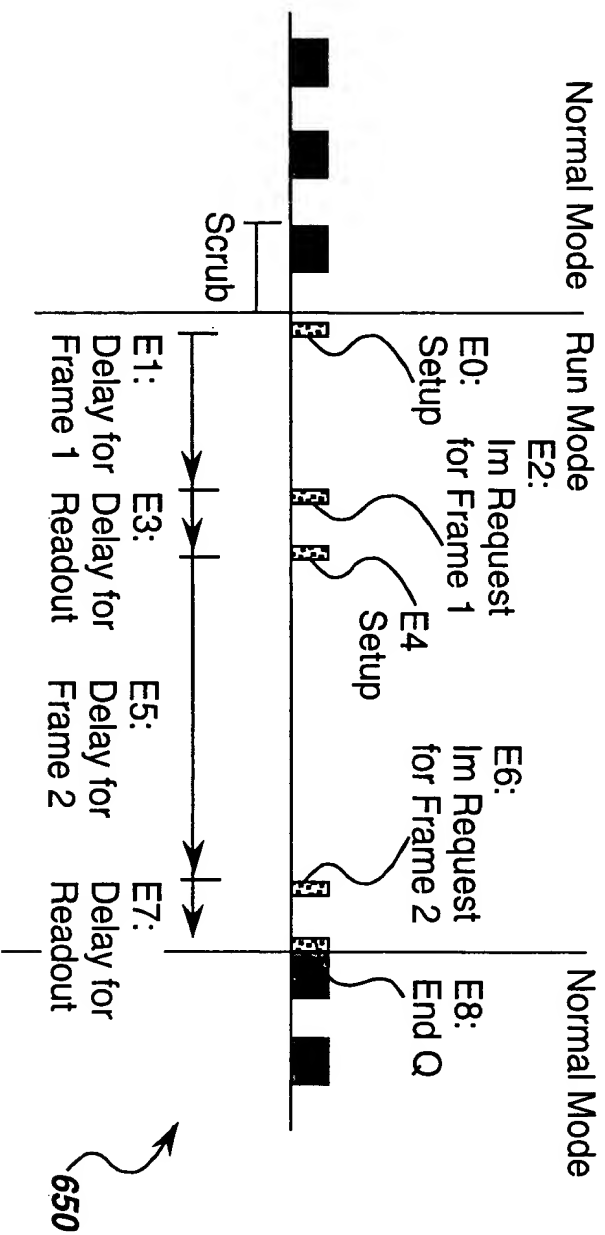


fig. 49

<i>Event Mnemonic</i>	<i>Event</i> (showing size of arguments)	<i>Op Code</i> (hex)	<i>Data</i> (bytes)	<i>Total</i> (bytes)
Endq	Endq	14	0	1
Delay (T)	Delay (0x $\text{ff ff ff ff}$ )	10	4	5
Send (command, value)	Send (0x $\text{ff ff ff ff}$ , 0x $\text{ff ff ff ff}$ )	04	8	9
LoopKN (K, N)	LoopKN (0x $\text{ff ff}$ , 0x $\text{ff}$ )	0C	3	4
LoopKF (K, F)	LoopKF (0x $\text{ff ff}$ , 0x $\text{ff ff ff}$ )	0D	5	6
Wait (F)	Wait (0x $\text{ff ff}$ , $\text{ff}$ )	09	3	4
Flag (F)	Flag (0x $\text{ff ff}$ , $\text{ff}$ )	08	3	4

660

fig. 50

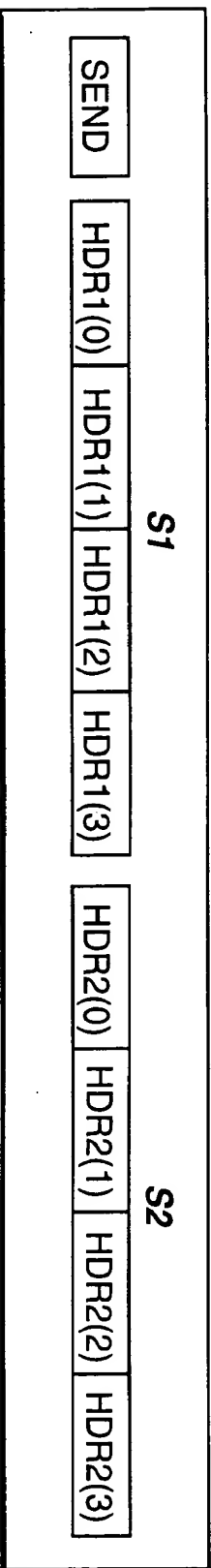


fig. 51

SEND

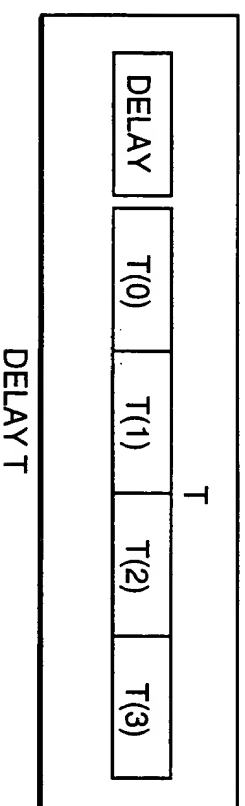
670

Error Mnemonic	Description of Error
FC_TIMEOUT	Timeout Expired With No ACK Detected
FC_BAD_ACK	ACK Did Not Match Transmitted Command
FC_EXTRA_ACK	Unexpected ACK Received
FC_EXTRA_CMD	New Send Event While Waiting for ACK From Previous Send
SIG_DET_N	No Input Signal Power on Fibre Channel (Cable Disconnected?)
RXERROR	Fibre Channel Receiver Detected Bad Data (Defective Chipset?)
WRDSYNCHN	Fibre Channel Data Link Unsynchronized
CRXS(1)	Bad Received CRC Detected (Fiber-optic Cable Problem?)
CRXS(3) & CRXS(2)	Bad Order in Link State Machine (Defective Chipset?)

672

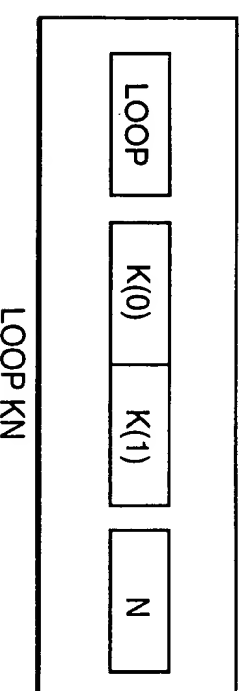
fig. 52

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fig. 53



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fig. 54

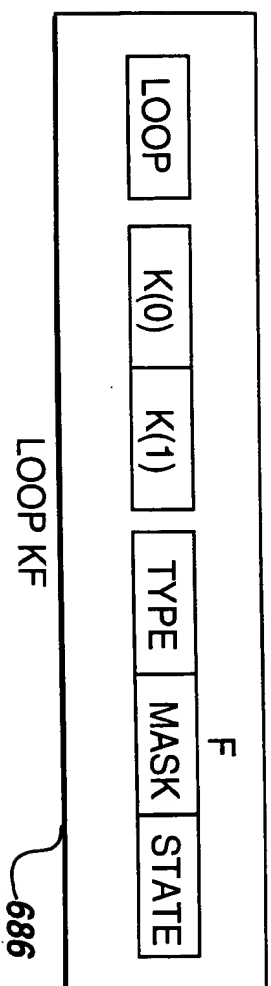


fig. 55

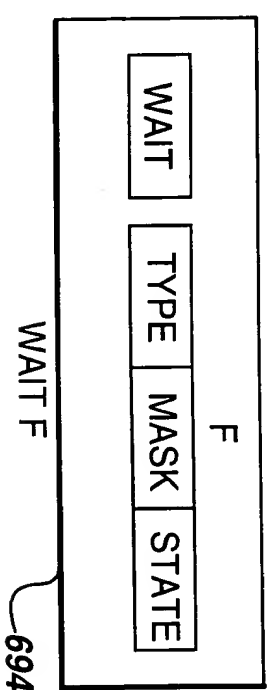


fig. 56

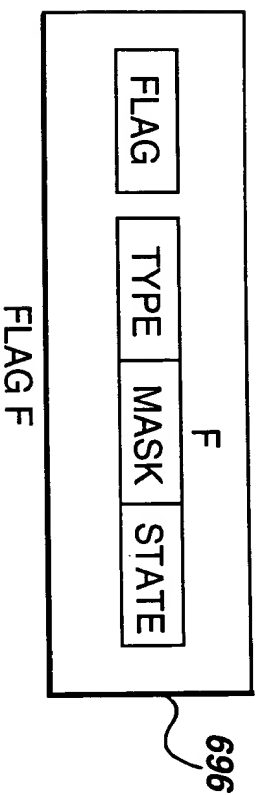


fig. 57

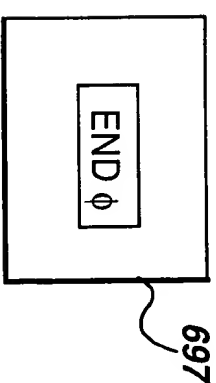


fig. 58

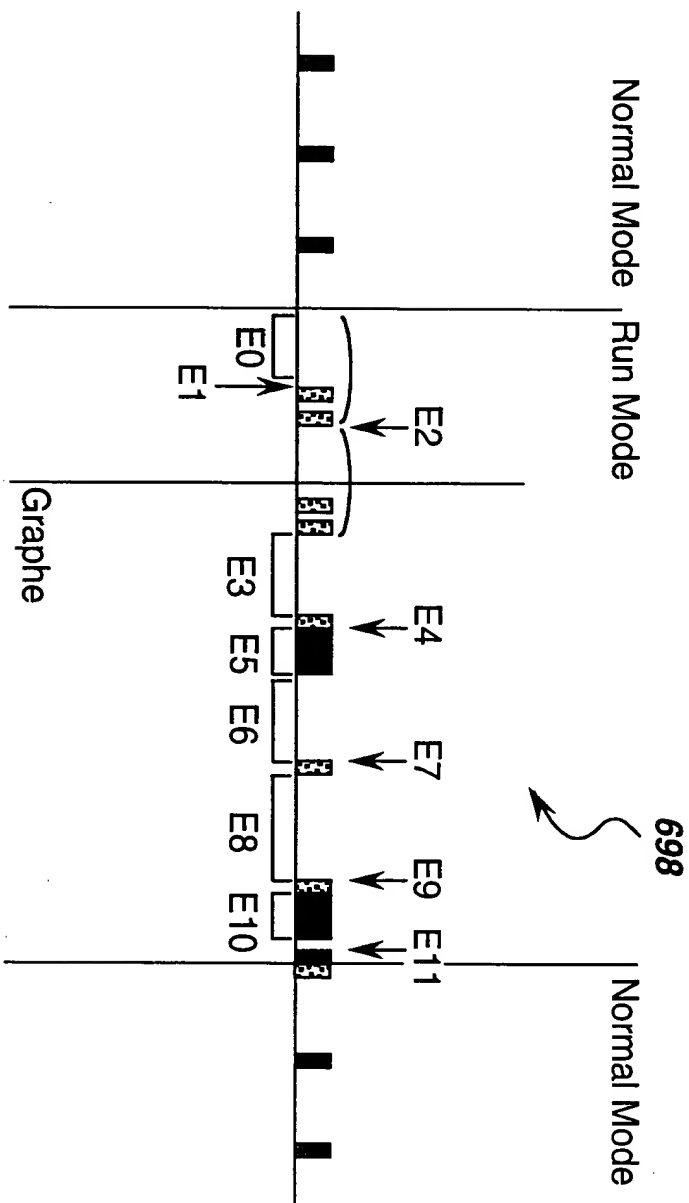


fig. 59

fig. 60

E11	EndQ
E10	Delay 125 ms
E9	Send Im Request
E8	Delay 500 ms
E7	Flag RT2
E6	Delay 50 ms
E5	Delay 125 ms
E4	Send Im Request
E3	Delay 300 ms
E2	Loop 2, RT1
E1	Send Scrub
E0	Delay 300 ms

EVENT QUEUE

700

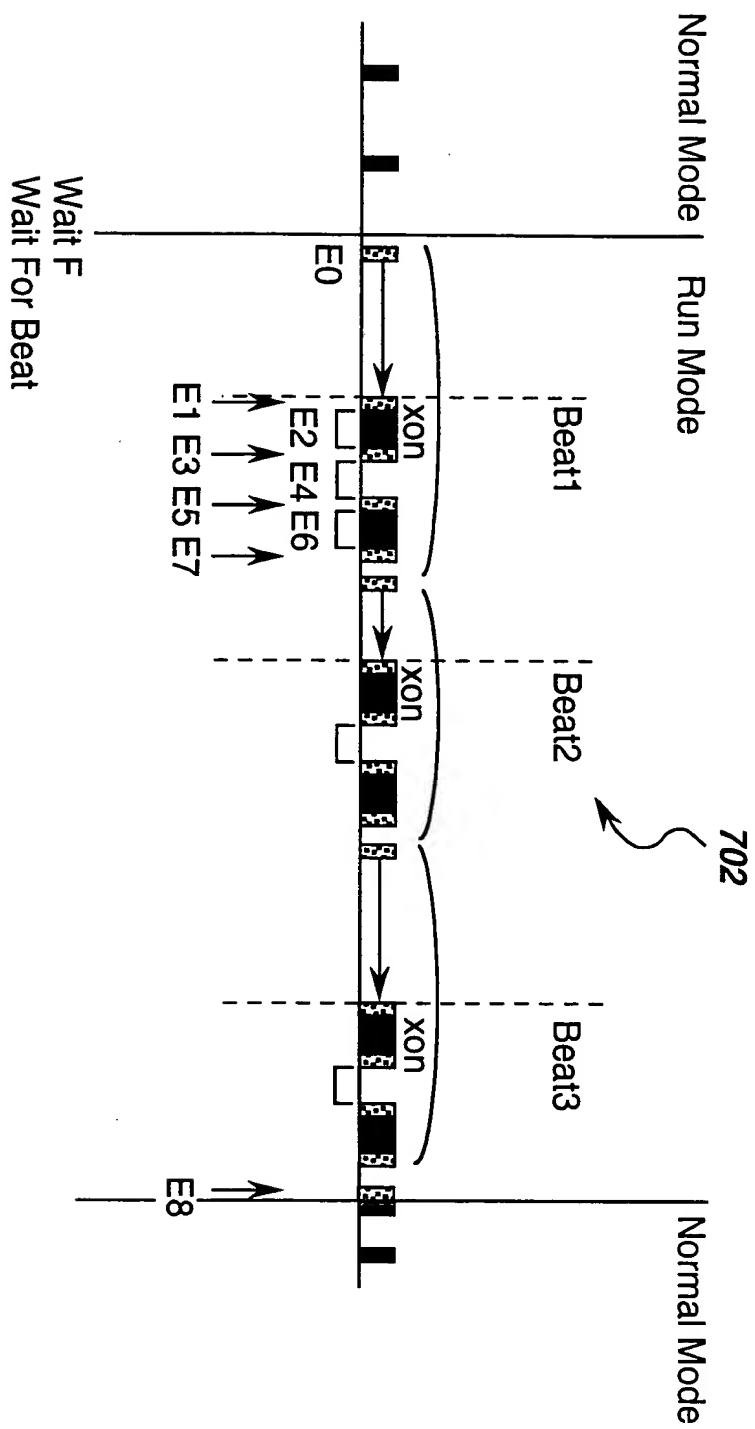
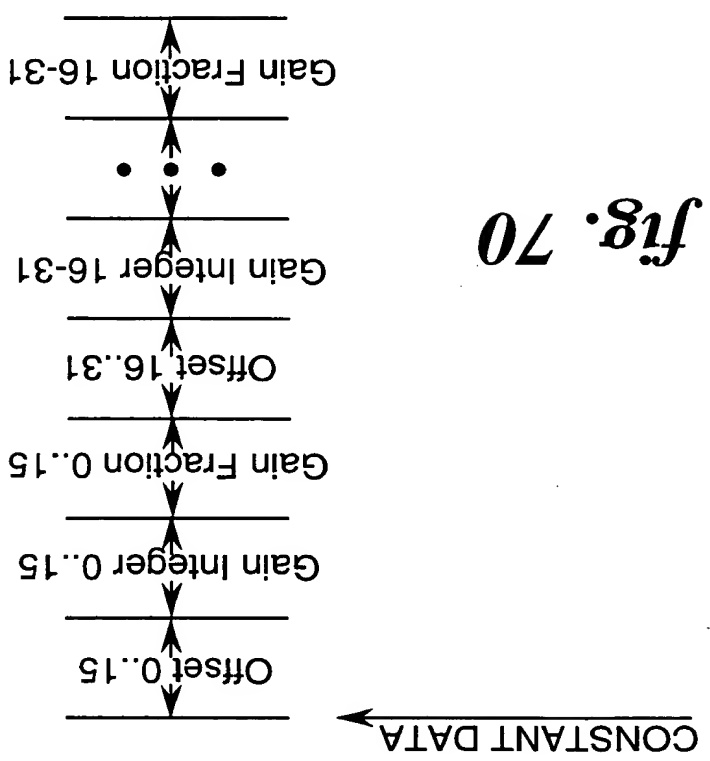


fig. 61



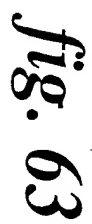
**fig. 62**

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E0	Wait RT1
E1	Send Scrub Request
E2	Delay 23 ms
E3	Flag RT2
E4	Delay 10 ms
E5	Send Im Request
E6	Delay 23 ms
E7	LoopKF, HF1
	EndQ

EVENT QUEUE





```
sequence_begin ( );
# define qv defaults:
%qv1 =( 'delay_qv' => 5000);
# call frame with qv's
frame_type1(NULL, \%qv1, 1);
sequence_end ( );
```

*fig. 64*

```
sub frame
{
$QVf = 'frame';
%qv = ( 'delay_qv' => [10000]);
%qp = ( );
compile_init ( @_, \%qp, \%qv, $QVf);
    Delay('Delay_qv1');
compile_finit ( );
}
```

*fig. 65*

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```
pDFN->DFNChangeQueueVariable
(
(char *) SymName,           // variable name
(char *) sndBuf,           // new value
BufSize                    // num bytes to write
(ULONG *) & Debug         // developer info
);
```

*fig. 66*

```
// load and run the event sequence
pDFNBeginSequenceNoMappingNoLog
(snum,"d:\\HF.bin");
// assign data to be passed
sndBuf = 25000;

// change the queue variable
pDFN->DFNChange QueueVariable
(
    (char *) SymName,           // variable name
    (char *) sndBuf,           // new value
    (ULONG ) sizeof sndBuf     // num bytes to write
    (ULONG *) & debug         // developer info
);
```

fig. 67

fig. 68

```
sub frame_type1
{
    $HFfirm = 'frame_type1';
    %qv = ('delay_qv' => [20000]);
    %qp = ();
    $image_cmd = [0x800000,0x0];
    compile_init (@_,\%qp,\%qv,$HFfirm);
    Send ($image_cmd);
    Delay('delay_qv');
    LoopKF(2, 0xAAFF01);
    compile_finit();
}
```

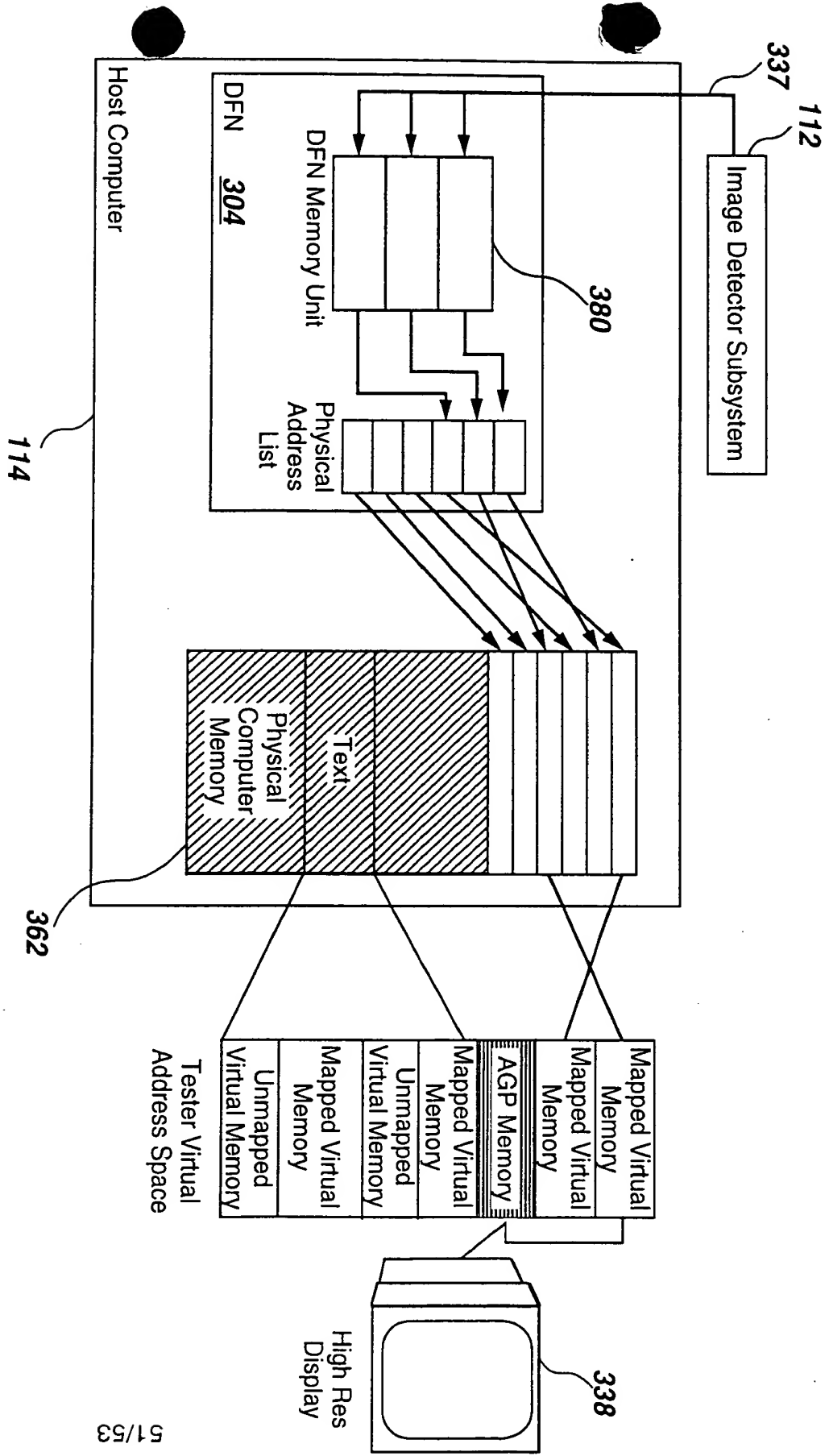


fig. 69

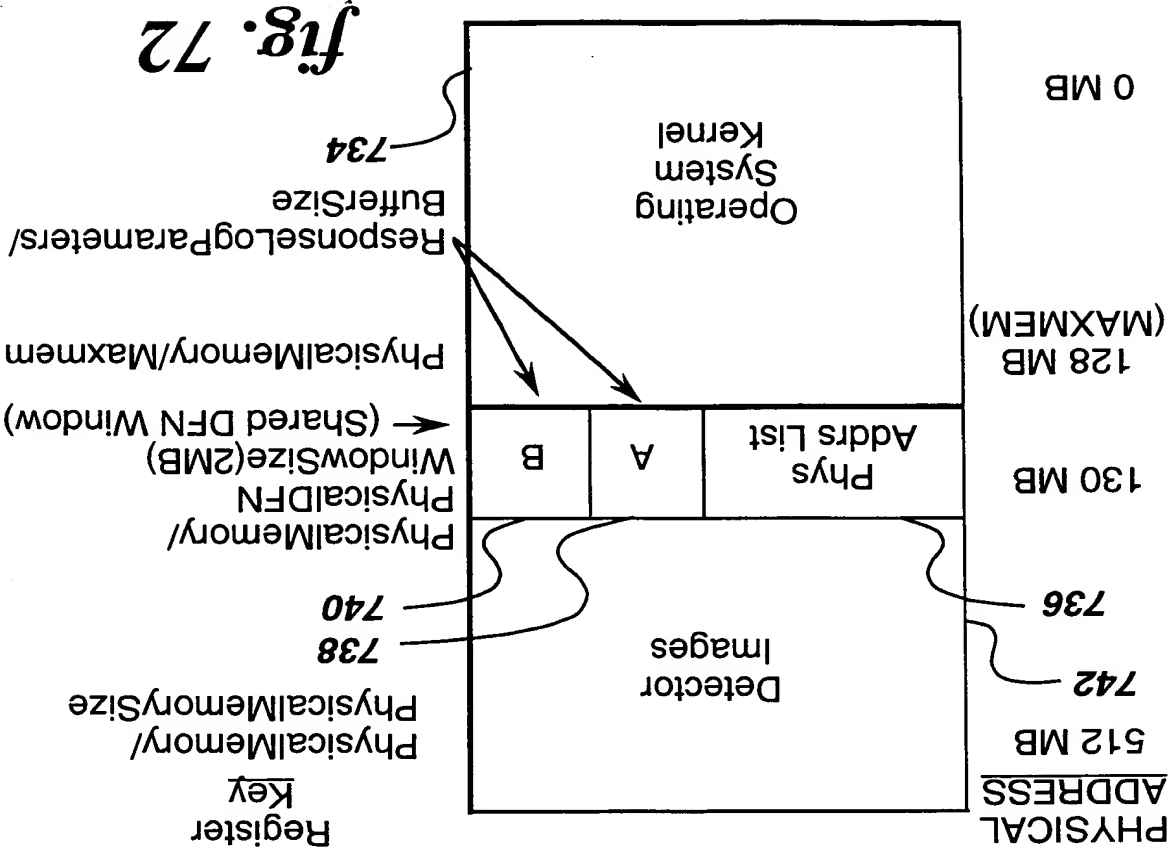


fig. 72

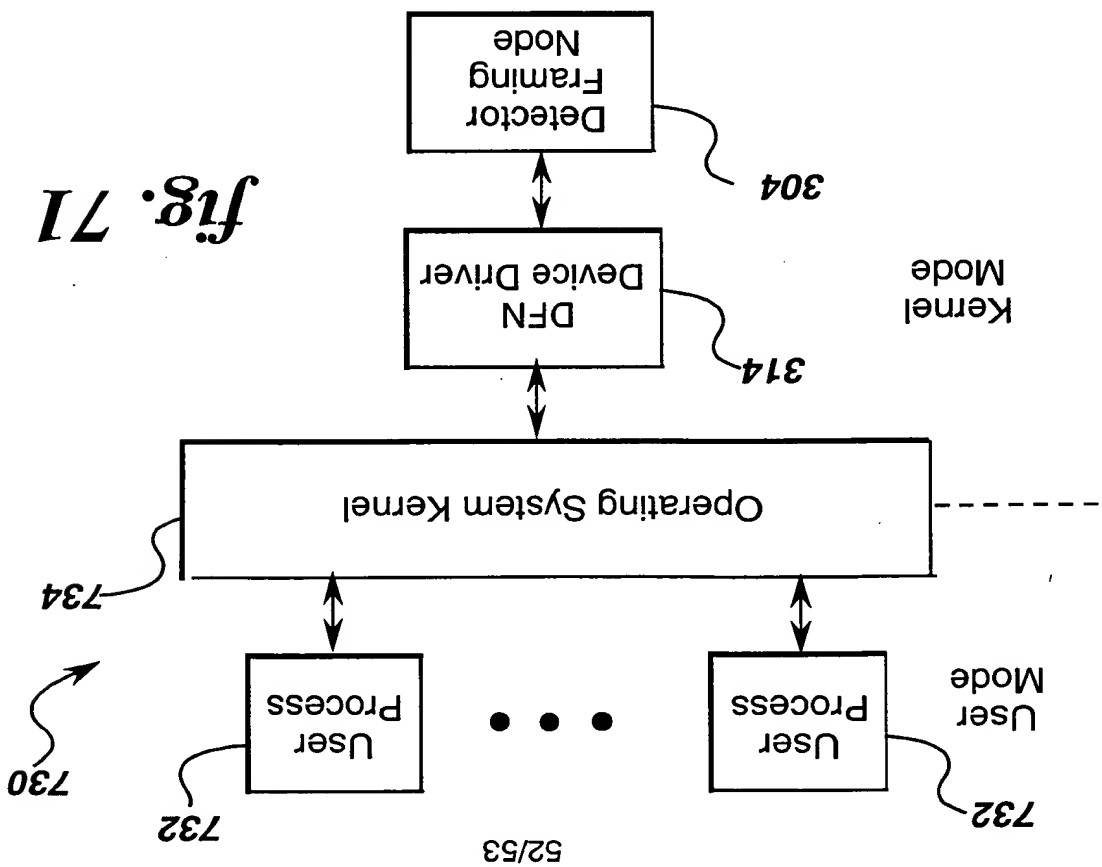


fig. 71

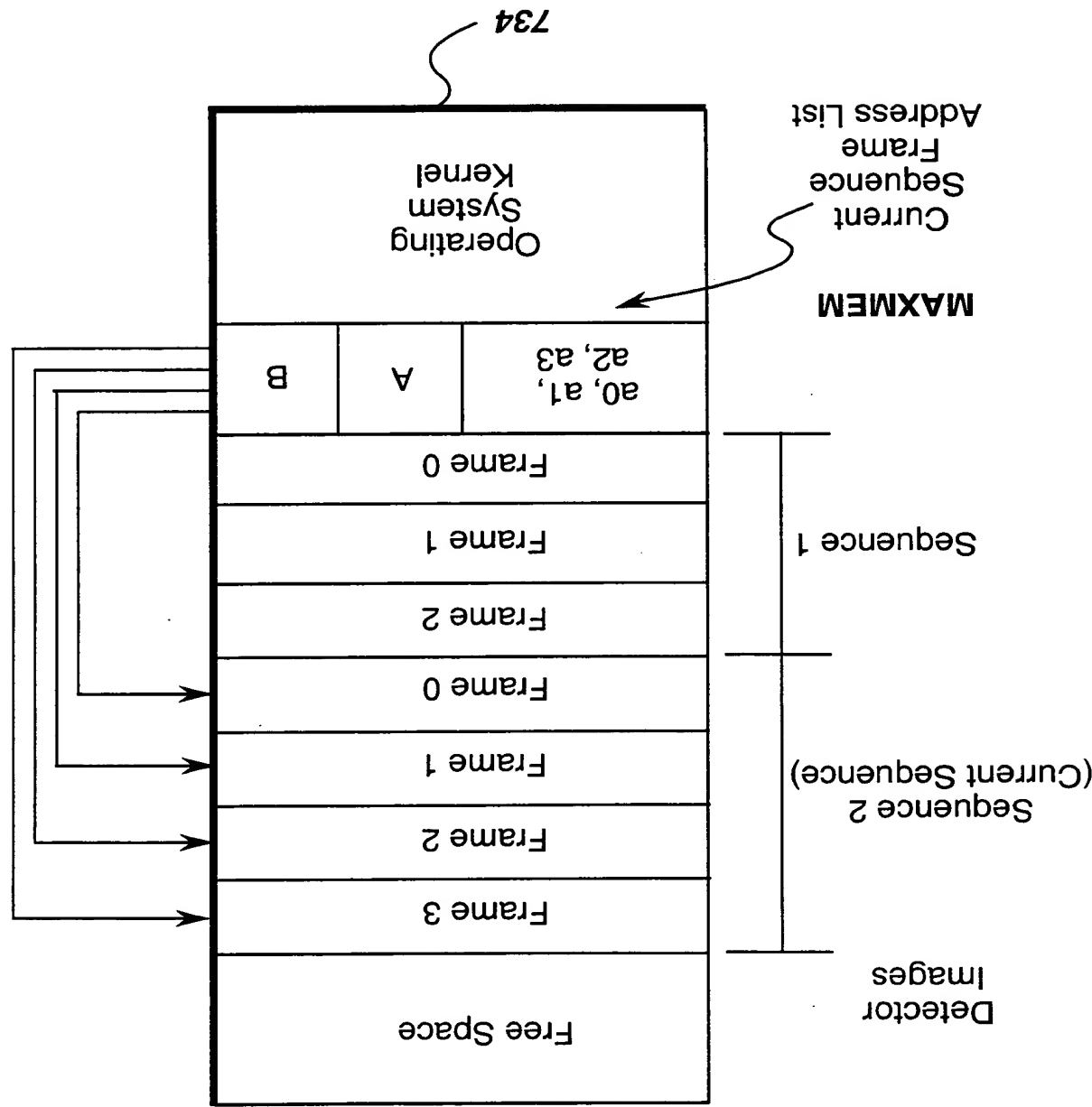


fig. 73